Design of Low Power Hearing Aid Processors

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Contents

- Hearing loss and modern hearing aids
- Concept of an Application Specific Instruction-Set Processor
- How to improve hearing aids with ASIPs
- The KAVUAKA ASIP architecture
- Current trends in hearing aid processor design
- Conclusion
Nicht sehen können trennt von den Dingen, nicht hören können von den Menschen.

Immanuel Kant

Quelle: wikimedia.org
Hearing Loss in modern Society

- Social interaction is based on communication
- Hearing loss is one of the most common sensoric deficits and often unknown or untreated

"https://www.preciosahome.com/buddha-bar/"
Perceptual Range of Hearing

- Painfully Loud
- Pain threshold
- Perception threshold
- Not noticeable
- Frequency kHz
- Sound level dB
Hearing Loss in the Outer and Middle Ear

- Conductive hearing loss
  - Blockage of the ear canal
  - Damage or infection in the middle ear

- Sensorineural hearing loss
  - Damage to the cochlea
  - Damaged auditory nerve

Quelle: https://www.hoersysteme.ch
Hearing Loss in the Inner Ear and Brain

- Neural hearing loss
  - Damaged auditory nerve (non-genetic or genetic reasons)
- Central hearing loss
  - Disturbed perception processing of auditory stimuli in the brain

Quelle: https://www.hoersysteme.ch
Hearing Aids against Hearing Loss

- Hearing aids can compensate for hearing loss in many cases
- An individual adjustment to the needs and complaints of a user is necessary and possible.
Hearing Loss and Hearing Aids

- From 2000 to 2015, the number of Americans with hearing loss has doubled. Globally the number is up by 44%. [1]
- Reduced speech intelligibility in complex acoustic scenarios with noise
- The consequences are difficulties with social interaction and at work
- Treatment: Hearing aid devices

Cochlear Implant

- Consisting of 2 components
  - Processor
  - Implant
- Processor usually worn behind the ear
- Implant placed under the skin
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Market shares of the largest hearing aid companies

- Market volume: ~6 billion US dollars

Quelle: Finanz und Wirtschaft (Schweiz)
Cochlear Implant Manufacturer

- Market volume: ~3 billion US dollars
Signal Processing in High-End Hearing Aids Systems

Example of Audiogram

Classification
knowledge
knowledge

Feature
classification
algorithm
situation
parameter
selection

Directional microphone
omni-directional

Feedback suppression

Analysis
Noise reduction
Amplification
(incl. Dynamic compression)
Synthesis
filterbank

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Seminar Processor Design, December 11, 2020
Digital Hearing Aid Systems

- Hearing aid technology requirements
  - Low-power: \(~1 \text{ mW}\) (longer battery lifetime)
  - Low processing delay: \(<10 \text{ ms}\)
  - Small form factor (higher user acceptance)
  - Processing performance (algorithms)
  - Programmability / flexibility
Application Specific Instruction-Set Processor for Hearing Aids

- Exploring the application specific instruction set processor concept for hearing aid systems
  - ISA, data path width, pipelining, ...
- Evaluating low-power hardware accelerators and design methodologies
  - Co-processors, custom hardware, ...
- Power Optimization
  - Power modeling and power-aware compiler/scheduler techniques
Low-Power Hearing Aid ASIPs

RISC Processor

\[ A_a \]

Real-Time Processing Constraints (\( t_c \))

\[ f_a = \frac{N}{t_c} \]

\[ P_{dyn,a} = \sigma \cdot f_a \cdot C_a \cdot U^2 \]

RISC Processor

\[ A_b = 2 \cdot A_a \]

Real-Time Processing Constraints (\( t_c \))

\[ f_b = \frac{1}{4} \cdot f_a \]

\[ P_{dyn,b} = \frac{1}{2} \cdot \sigma \cdot f_a \cdot C_a \cdot U^2 \]
Application Specific Instruction-Set Processor

- Baseline Architecture
Application Specific Instruction-Set Processor

- Baseline Architecture
- Basic Architecture Parameters
  - Register File Configuration
  - Memory System
  - Instruction-Set Architecture
- Parallelization Techniques
  - Number of Parallel Instructions
  - SIMD / Subword Parallelism
- Specialization Techniques
  - Custom Instructions
  - Co-processor Architectures
- Compiler / Software Support
Xtensa Customizable Processor / Cadence

- **Baseline Architecture**
  - Reduced 32-bit ISA, 5 pipeline stages
  - 16 KB Instruction Cache and 16 KB Memory Cache
- **Configurable**
  - Caches, bus width, GP register file, MUL, MAC, INT, number of load/store units
- **Expandable**
  - New instruction, register, ports
  - Using TIE language (similar to Verilog)

- Area and energy optimization are possible
Extension of the Xtensia Processor with hardware units

- Using TIE language (Tensilica Instruction Extension)
  - Custom instructions, registers and interfaces
  - Can be used in the C program code
  - SIMD-example: 4x 16bit additions

```c
#include <xtensa/tie/vec4_add16.h>
simd64 A[VECLEN];
simd64 B[VECLEN];
simd64 sum[VECLEN];
for (i=0; i<VECLEN; i++)
  sum[i] = vec4_add16(A[i],B[i]);
```

**Definition of a custom instruction**

```c
define vec4_add16
```
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**Xtensa Customizable Processor / Cadence**

- Configuration Implemented for the HA System
  - Baseline (1-Issue-Slot)
  - Baseline (2-Issue-Slots)
  - Baseline (3-Issue-Slots)
  **Exploring parallelism**

- Customized (1-Issue-Slot)
  **Exploring specialization**

- Customized (2-Issue-Slots)
  **Exploring parallelism and specialization**
Customized Configuration: Complex Instruction Extensions

- Analysis Filterbank
- Noise Reduction
- Amplification (incl. Dynamic compression)
- Synthesis Filterbank

Total number of cycles per Audio Buffer:
- 50% FFT
- 65% SQRT
- 50% IFFT

Overlap+Add
Customized Configuration: Complex Instruction Extensions

Customized Configuration: Complex Instruction Extensions

  - $R0 = \text{COMPLEX}\_\text{ADD}(R1,R2)$
  - $R0 = \text{COMPLEX}\_\text{MUL}(R1,R2)$
  - $R0 = \text{COMPLEX}\_\text{CONJ}(R1)$
  - $AR0 = \text{BIT}\_\text{REVERSE}(AR1)$

![Diagram of register file and complex arithmetic operations]

![Graph of total number of cycles per audio buffer]

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Customized Configuration: Complex Instruction Extensions

  - \( R_0 = \text{COMPLEX\_ADD}(R_1, R_2) \)
  - \( R_0 = \text{COMPLEX\_MUL}(R_1, R_2) \)
  - \( R_0 = \text{COMPLEX\_CONJ}(R_1) \)
  - \( AR_0 = \text{BIT\_REVERSE}(AR_1) \)

![Diagram of Register File](image)

**Register File (each Register 64-Bits)**

<table>
<thead>
<tr>
<th>Register</th>
<th>C.real</th>
<th>C.img</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0</td>
<td>A.real</td>
<td>A.img</td>
</tr>
<tr>
<td>R1</td>
<td>B.real</td>
<td>B.img</td>
</tr>
<tr>
<td>R2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Diagram of Arithmetic Operations**

- \( \text{ADD} \)
- \( \text{MUL} \)
- \( \text{SUB} \)
- \( \text{ADD} \)

**Graph of Total Number of Cycles per Audio Buffer**

- Analysis Filterbank: 5000 cycles
- Noise Reduction: 10000 cycles
- Amplification: 15000 cycles
- Synthesis Filterbank: 20000 cycles

*65% SQRT reduction*
Customized Configuration: Complex Instruction Extensions

- **SQRT Operations**
  - LEADING_ONES(R0)
  - \( R0 = SQUARE\_ROOT(R1) \)
  - \( R0 = THRESHOLD(R0,R1,R2) \)

Newton-Raphson method for square root computation

![Graph showing total number of cycles per Audio Buffer for different stages](image)

- Analysis Filterbank: x16 reduction, 65% SQRT
- Noise Reduction: negligible
- Amplification: negligible
- Synthesis Filterbank: negligible

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Exemplary Hearing Aid Processing - ASIP Design Space Exploration

These estimations are done for a 40 nm low power technology process.

[Werner; Payá Vayá, Blume, “Case Study: Using the Xtensa LX4 Configurable Processor for Hearing Aid Applications”, ICT.OPEN 2013]
Exemplary Hearing Aid Processing - ASIP Design Space Exploration

These estimations are done for a 40 nm low power technology process.
Baseline KAVUAKA Architecture

- **ASIP Processor Architecture**
- **Basic Generic Parameters**
  - Pipeline Stages
  - Bitwidth (64/48/32/24 bit)
- **Parallelization Techniques**
  - SIMD Subword Parallelism
  - VLIW Instruction Parallelism
- **Specialization Techniques**
  - Complex-valued MAC
  - Co-Processors
  - Instruction Merge (X2)
  - Idle Operation
- 4 configurations selected for the SoC
KAVUAKA Hearing Aid Processor System-on-Chip

- The manufactured KAVUAKA hearing aid System-on-Chip
  - 40 nm TSMC LP technology
  - 3.6 mm² chip area
  - 0.8 million standard cells
  - 28 SRAM memories
    - 4x 2048x64-bit
    - 4x 1024x64-bit
    - 4x 1024x48-bit
    - 16x 512x16-bit
  - 37 input/output cells
  - 8 metal layers

Close-up of the chip with approx. 125x magnification.
### KAVUAKA ASIP configurations

<table>
<thead>
<tr>
<th>SIMD instructions</th>
<th>CMAC (CMAC)</th>
<th>Instruction Merge (X2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1x64 bit, 2x32 bit, and 8x8 bit</td>
<td>Functional units duplicated</td>
</tr>
<tr>
<td></td>
<td>2x24 bit, 4x12 bit</td>
<td>Load/Store up to 256 bit</td>
</tr>
<tr>
<td></td>
<td>4x12 bit</td>
<td>Functional units duplicated</td>
</tr>
<tr>
<td></td>
<td>4x12 bit</td>
<td>Load/Store up to 192 bit</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Scalar instructions</th>
<th>Standard MAC</th>
<th>No Instruction Merge</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1x32 bit</td>
<td>Load/Store up to 64 bit</td>
</tr>
<tr>
<td></td>
<td>1x24 bit</td>
<td>Load/Store up to 48 bit</td>
</tr>
</tbody>
</table>
Co-Processor Architecture

- Co-Processor Architecture
  - CORDIC (Coordinate Rotation Digital Computer)
- Generic parameters
  - Number of CORDIC kernel processing units
  - Single instruction multiple data (SIMD) operations

➢ 10 configurations selected for the SoC

Example applications:
- Division: Normalized LMS Algorithm (Beamforming)
- Logarithm: Log power spectrum (Speech recognition)
The System-on-Chip Architecture

System-on-Chip
with
4 KAVUAKA
cores and
10 co-processors
In-circuit Emulation of KAVUAKA

- Functional verification of the SoC
- Use real or emulated external components
- ASIC is placed on the test socket after tape-out
Setup for Power Measurements

- Measure the power consumption for different hearing aid configurations and algorithms
- Automatic measurements including:
  - Host PC for controlling and audio streaming
  - Power supply and oscilloscopes controlled by PC
  - FPGA emulation of external hearing aid components
Beamforming Algorithms for Hearing Aids

Fixed Beamformer

Adaptive Gain Beamformer

Adaptive Filter Beamformer
Results for Beamforming Algorithms on different ASIP configurations

- Fixed and adaptive Beamforming algorithms
- 4 ASIP configurations
- Power and area evaluation

![Graph showing power consumption in mW for different configurations.](image-url)

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Power Consumption in mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>24-bit</td>
<td>0.00</td>
</tr>
<tr>
<td>32-bit</td>
<td>0.20</td>
</tr>
<tr>
<td>48-bit +SIMD</td>
<td>0.42</td>
</tr>
<tr>
<td>64-bit +SIMD</td>
<td>2.91</td>
</tr>
</tbody>
</table>

![Diagram showing 64-bit SIMD Processor and 48-bit SIMD Processor configurations.](image-url)
Power Optimization Based on an Accurate Power Model

- Power optimization after manufacturing
- Exploit the flexibility offered by the ASIP architecture
  - During instruction scheduling and register allocation
- Register accesses cause high switching activity in the address decoder of the multi port register file

Register addressing of two consecutive instructions influences power consumption

<table>
<thead>
<tr>
<th>Worst Case:</th>
<th>Best case:</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD R0, R0, R0</td>
<td>ADD R0, R0, R0</td>
</tr>
<tr>
<td>ADD R31, R31, R31</td>
<td>ADD R0, R0, R0</td>
</tr>
</tbody>
</table>

Graph showing total power consumption for worst and best cases with a decrease of 7.87%
Feature Sizes of Commercial and Research Hearing Aids

- Hard-wired w/ an analog front end
- ASIP w/ an analog front end
- ASIP+accelerators w/ an analog front end
- Hard-wired w/o an analog front end
- ASIP w/o an analog front end
- ASIP+accelerators w/o an analog front end

Smart Hearable
28 nm

KAVUAKA
40 nm

Processor With CNN FFT Accelerators
Power Consumption of Commercial and Research Hearing Aids

- Hard-wired w/ an analog front end
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Smart Hearable
28 nm
Processor With CNN FFT Accelerators

KAVUAKA
40 nm
Silicon Area of Commercial and Research Hearing Aids

- Hard-wired w/ an analog front end
- ASIP w/ an analog front end
- **ASIP+accelerators** w/ an analog front end
- Hard-wired w/o an analog front end
- ASIP w/o an analog front end
- **ASIP+accelerators** w/o an analog front end

- Smart Hearable
  - 28 nm
- Processor With
  - CNN FFT
  - KAVUAKA
  - 40 nm
On-Chip Memory Sizes

On-Chip Memory Sizes in kB

- EZAIRO 7111
- HYBRID: Audio Processor
- KAVUAKA
- Processor With CNN FFT Accelerators

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Smart Hearing Aid Processor (SmartHeaP) ASIC Concept

Reference algorithms

22 nm FDSOI
Applied Deep Learning in Hearing Aids

- Cocktail Party Scenario: many Speakers and Noise
- Advanced techniques available e.g. Beamformers, but Direction of Arrival (DOA) as input is needed [ICASSP 2020]
- Use CNN to estimate DOA of Speech
Conclusion

- Number of hearing impaired persons increases
  - New hearing aids are necessary
- Strict constrains, like power consumption or processing performance
- KAVUAKA - a hearing aid ASIP from the IMS
  - Design process and verification
  - Post silicon evaluation and optimization
- Further trends in hearing aid research
  - Accelerators for neural networks
  - EEG signal processing