

## Invitation to a talk

**Title:** Comparing Voltage Adaptation Performance between  
Replica and In-Situ Timing Monitors

**Presenter:** Professor Masanori Hashimoto, Ph. D., Osaka University, Japan



**Time, place:** Thursday, September 20, 2018, 17:00, room 4905

[https://portal.mytum.de/campus/roomfinder/search\\_room\\_results?searchstring=4905&building=0509&search=Suche+starten](https://portal.mytum.de/campus/roomfinder/search_room_results?searchstring=4905&building=0509&search=Suche+starten)

### Abstract:

Adaptive voltage scaling (AVS) is a promising approach to overcome manufacturing variability, dynamic environmental fluctuation, and aging. This talk focuses on timing sensors necessary for AVS implementation and compares in-situ timing error predictive FF (TEP-FF) and critical path replica in terms of how much voltage margin can be reduced. For estimating the theoretical bound of ideal AVS, this work proposes linear programming based minimum supply voltage analysis and discusses the voltage adaptation performance quantitatively by investigating the gap between the lower bound and actual supply voltages. Experimental results show that TEP-FF based AVS and replica based AVS achieve up to 13.3% and 8.9% supply voltage reduction, respectively while satisfying the target MTTF. AVS with TEP-FF tracks the theoretical bound with 2.5 to 5.6 % voltage margin while AVS with replica needs 7.2 to 9.9 % margin.

### Bio:

Masanori Hashimoto received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1997, 1999, and 2001, respectively. Now, he is a Professor in the Department of Information Systems Engineering, Osaka University, Osaka, Japan. His current research interests include design for manufacturability and reliability, timing and power integrity analysis, reconfigurable computing, soft error characterization and low-power circuit design. Dr. Hashimoto was a recipient of the Best Paper Award at ASP-DAC 2004. He was on the technical program committees of international conferences including DAC, ICCAD, ITC, Symposium on VLSI Circuits, ASP-DAC and DATE. He serves/served as an associate editor for IEEE TVLSI, TCAS-I, ACM TODAES and Elsevier Microelectronics Reliability.