Content

Computing increase and power challenge in (embedded) computing
- Heterogeneous multi-core architectures with dedicated accelerators
- New paradigm e.g. invasive computing

New Challenges
- Memory and bandwidth

Metrics for design space exploration
- Wireless baseband processing
- Impact of memories and data transfers on metrics
- Impact of application (communications) performance on metrics

3D MPSoCs
- 3D memories and memory controllers
New cellular mode is added every 3 years
A new frequency band is added every year
Continuous demand for higher data rates and more services

Communication Centric World

Baseband Receiver Structure

PARAMETER ESTIMATION
SIGNAL DETECTION
De-Interleaver
CHANNEL DECODER
RF&ADC
FRONT END
INNER RECEIVER
OUTER RECEIVER
3.5G Digital Workload (100GOPS@1Watt)

Future: 1 TOPS in 1+ Watt

Mobile Phone Trends – Inner Receiver

Source: Kees van Berkel, MPSoC2010
Mobile Phone Trends – Outer receiver

Throughput

- cdma2000
- wcdma
- td-SCDMA
- UMTS
- GPRS
- UMTS HSDPA
- UMTS EVA
- GSM
- LTE
- WCDMA
- TD-SCDMA
- UWB

Operations/Bit

- 0.1 GOPS
- 10 GOPS

- Cellular decoders
- Broadcast decoders
- Connectivity decoders

Bit rate [Mbps]

Source: Kees van Berkel, MPSoC 2010

3G $\leftrightarrow$ 3.9G (LTE): 130 x decoding Mops/mW

Music Baseband SDR Chip @ 65nm

Source: Infineon
**Metric – Energy Efficiency**

Example - SODA, DSP and GP Architectures
**Metric Assessment - Channel Decoders**

All architectures based on standard synthesis flows, 65nm technology@worst case, all data in-house available

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>ASIP (Magali)</td>
<td>Conv. Codes</td>
<td>N=16k</td>
<td>40</td>
<td>385</td>
<td>0.7</td>
<td>~100</td>
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<tr>
<td></td>
<td>Binary TC</td>
<td></td>
<td>14/16(6iter)</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Duo-binary TC</td>
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<td>38(6iter)</td>
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<tr>
<td>LTE Turbo</td>
<td>LTE turbo code</td>
<td>N=18k</td>
<td>150</td>
<td>300</td>
<td>2.1</td>
<td>~300</td>
</tr>
<tr>
<td>(Music)</td>
<td></td>
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<td>(6iter)</td>
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<tr>
<td>LDPC flex</td>
<td>R=1/4 to R=9/10</td>
<td>N=16k</td>
<td>150 to 300</td>
<td>385</td>
<td>1.72</td>
<td>~389</td>
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<tr>
<td>(Magali)</td>
<td></td>
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<td>(20-100iter)</td>
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<tr>
<td>LDPC fixed</td>
<td>R=3/4</td>
<td>N=1.2k</td>
<td>480</td>
<td>435</td>
<td>0.583</td>
<td>~202</td>
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<tr>
<td>(Magali)</td>
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<td>(6iter)</td>
<td></td>
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<tr>
<td>LDPC</td>
<td>R=1/2-4/5</td>
<td>N=1.3k</td>
<td>640</td>
<td>265</td>
<td>0.51</td>
<td>~193</td>
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<td>WiMedia 1.5</td>
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<td></td>
<td>(R=1/2,5iter)</td>
<td></td>
<td></td>
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<tr>
<td></td>
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<td></td>
<td>960 (R=3,5iter)</td>
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<tr>
<td>CC Decoder</td>
<td>64-state NSC</td>
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<td>500</td>
<td>500</td>
<td>0.1</td>
<td>~37</td>
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**Algorithmic Throughput Calculations [GOPs]**

<table>
<thead>
<tr>
<th>Code</th>
<th>Operations per decoded information bit normalized to ~8bit addition</th>
<th>Infobit-Throughput @8bit operations per second (GOPs)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>100Mbit/s 300Mbit/s 1 Gbit/s</td>
</tr>
<tr>
<td>CC: states=64</td>
<td>~200</td>
<td>~20</td>
</tr>
<tr>
<td>LDPC Min-Sum</td>
<td>5 iter 75/R</td>
<td>~7.5/R</td>
</tr>
<tr>
<td></td>
<td>10 iter 150/R</td>
<td>~15/R</td>
</tr>
<tr>
<td></td>
<td>20 iter 300/R</td>
<td>~30/R</td>
</tr>
<tr>
<td></td>
<td>40 iter 600/R</td>
<td>~60/R</td>
</tr>
<tr>
<td></td>
<td>(x3.4 appr. BP)</td>
<td>~105/R</td>
</tr>
<tr>
<td>Turbo Max-Log</td>
<td>2 iter 280</td>
<td>~28</td>
</tr>
<tr>
<td></td>
<td>4 iter 560</td>
<td>~56</td>
</tr>
<tr>
<td></td>
<td>6 iter 840</td>
<td>~84</td>
</tr>
</tbody>
</table>
Area- and Energy Efficiency

What about Memory/Data Transfers

Current metric: energy efficiency = only operations/energy
Data transfers/ accesses substantially contribute to the power consumption

Example (R=0.5)
150 Mbit/s Turbo : ~126 Gops  ~40 Gaccesses
150 Mbit/s LDPC : ~90 Gops  ~80 Gaccesses

Efficient data transfer is key for efficient implementation
- LTE TC: special interleaver structure to avoid access conflicts
- DVB-S2/WiMAX LDPC: special code structure to minimize access conflicts

Efficiency metrics based on operations only are not appropriate
- Power includes operations and accesses!
- Architectures are favored where operations dominate compared to accesses
**Decoders in System Design Space**

Overall efficiency of a baseband receiver depends on:
- Implementation performance
- Communications performance
- Flexibility

**Scenario 1: Fixed Communication performance**
- Comparison of two iterative decoders with same communications performance but different parameters (codes, code rate, iterations)
  - impact on implementation efficiency

**Scenario 2: Implementation driven**
- Comparison of iterative and non-iterative decoders with varying communications performance
- 64-state convolutional code 960 Mbit/s (WiMedia 1.2) and WiMedia 1.5 LDPC decoder
  - impact on implementations efficiency
Scenario 1: Fixed Communication Performance

Blocksize 6145 Information bits, TC: 150Mbit/s @6.5 iterations

Scenario 1: Implementation Efficiency

TC efficiency constant for all code rates, 6.5 iter
R=1/3, 40 iter
R=4/5, 10 iter
R=1/2, 20 iter

TC LTE
flexible LDPC
Scenario 2: Varying Communication Performance

Simulation Set-Up: WiMedia 1.5 chain, 16-QAM, Blocksize 1200 Information bits

Scenario 2: Implementation Efficiency

Area Efficiency: (Mbit/s)/mm²

Energy Efficiency: decoded bit/energy (bit/nJ)

- LDPC WiMedia 1.5
- CC WiMedia 1.5

- 4dB better com. Perf. (5iter)
  Identical throughput
- 4dB worse com. Perf. (1iter)
  5 times higher throughput
- Identical comm. Perf. (2iter)
- Identical throughput
- 4dB worse com. Perf. (1iter)
  Identical throughput
- 2.5 times higher throughput

100
1000
10000
100000

Area Efficiency: (Mbit/s)/mm²
Lessons learned

- Understanding trade-offs between implementation efficiency, application performance and flexibility requirements is mandatory for efficient baseband receivers.

- Operation based metrics for energy and area efficiency can be misleading.

- Memory and data transfers have to be considered in metrics for design space exploration.

- Implementation efficiency metrics have to be linked to application performance trajectory.

Off-chip Memory Bandwidth

\[ C = \frac{T}{B}^{\delta} \]

with \( \delta \approx 2-3 \)

Using Cache size to accommodate increasing traffic is VERY expensive!

2x increased traffic drives 8x cache size (constant memory bandwidth)

4x increased traffic drives 64x cache size (constant memory bandwidth B)

Source: IBM
Traditional JEDEC DRAM channels are saturating
3D Integration with TSVs

Through Silicon Vias (TSV)
- Polysilicon filled (FEOL)
  - 10,000 TSV/mm²
- Copper filled (BEOL)
  - 500 TSV/mm²

Source: LETI

Wide IO Technology (JEDEC Standard 2012)

Channel
- 4 x 64Mb
- 128 bit @ 200MHz SDR
- 3.2GBps

Memory
- 4 channels
- 1Gb
- 512 bit IO
- 12.8GBps

Source: LETI
Power Savings in DRAM Memory Interfaces

- Much wider I/Os possible >> 32 bits

<table>
<thead>
<tr>
<th>Memory link, peak bandwidth and power consumption efficiency</th>
<th>Cost for 1Tbps memory bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-core CPU ↔ DRAM 8.532 GBps 30 mW/Gbps</td>
<td>Number of data I/O pins Interface power consumption</td>
</tr>
<tr>
<td>1066 MHz I/O bus clock, 32 bits, 1.5 V, Double Data Rate</td>
<td>3800 240 W</td>
</tr>
<tr>
<td>Multi-core CPU ↔ DRAM 4.264 GBps 20 mW/Gbps</td>
<td></td>
</tr>
<tr>
<td>533 MHz I/O bus clock, 32 bits, 1.2 V, Double Data Rate</td>
<td>7700 160 W</td>
</tr>
<tr>
<td>Multi-core CPU ↔ DRAM 12.8 GBps 4 mW/Gbps</td>
<td></td>
</tr>
<tr>
<td>200 MHz I/O bus clock, 512 bits, 1.3 V, Single Data Rate</td>
<td>41000 32 W</td>
</tr>
</tbody>
</table>

Transition to 3D-DRAMs
Organization and Naming

A single 3D-layer consists of 3D-DRAM banks
A bank is composed of DRAM core tiles

3D-layer (= tier)

3D-DRAM bank

64Mb

3D-DRAM core tile

64Mb

Example: 64Mb 3D-DRAM core tile
- TSV areas added
- Deep trench / buried WL / Stack
- Cell sizes: 8F² – 4F²
- Based on measured* & simulated data

Investigated Technologies

<table>
<thead>
<tr>
<th>No.</th>
<th>Technology</th>
<th>Cell size</th>
<th>Cell type</th>
<th>Area [mm²]</th>
<th>Row 4t [ns]</th>
<th>Row → Col. 4t [ns]</th>
<th>Column 4t [ns]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>75nm</td>
<td>8F²</td>
<td>Deep Trench</td>
<td>5.20</td>
<td>39.0</td>
<td>9.30</td>
<td>6.05</td>
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<tr>
<td>2</td>
<td>65nm</td>
<td>6F²</td>
<td>buried WL</td>
<td>3.54</td>
<td>27.1</td>
<td>7.45</td>
<td>5.42</td>
</tr>
<tr>
<td>3</td>
<td>58nm</td>
<td>6F²</td>
<td>Stack</td>
<td>3.00</td>
<td>31.9</td>
<td>7.31</td>
<td>4.70</td>
</tr>
<tr>
<td>4</td>
<td>46nm</td>
<td>6F²</td>
<td>buried WL</td>
<td>2.26</td>
<td>26.4</td>
<td>6.44</td>
<td>3.59</td>
</tr>
<tr>
<td>5</td>
<td>45nm</td>
<td>4F²</td>
<td>buried WL</td>
<td>1.92</td>
<td>26.0</td>
<td>5.98</td>
<td>2.76</td>
</tr>
</tbody>
</table>
Single 3D-layer Design Space

- 1x 128Mb with 64 I/Os
- 2x 64Mb with 128 I/Os
- 4x 32Mb with 256 I/Os
- 8x 16Mb with 512 I/Os

Control / Voltage generators / Signaling
TSV area, I/Os, and Power

3D-DRAM models

Inputs:
- Number of 3D layers
- Number of log. banks
- DRAM size (Mbit)
- Data IO width
- IO width per base
- DDR or SDR interface
- Long or short bitlines
- Long or short wordlines
- TSV pitch and diameter
- Number of power TSVs
- Technology node

Outputs:
- Timings:
  - $t_{RC}$, $t_{RAS}$, $t_{CDD}$
  - $t_{DQ}$, $t_{RP}$, $t_{WR}$, ...
  - Max. frequency
- Power values:
  - Active (RD/WR)
  - Standby
  - Power down
  - Self refresh
- Area:
  - Per 3D layer

Cycle-accurate SystemVerilog/
SystemC simulation models
Metrics for Exploration

- **Throughput (TP)**
  - maximal theoretical bandwidth ($f_{\text{max}} \cdot$ IO width)
  - $f_{\text{max}}$ determined by architecture & technology
    - here: column to column access delay ($t_{\text{CCD}}$)

- **Area efficiency**
  - Maximum learning out of the commodity DRAM production: minimize cost/bit
  - Maximize cell efficiency (CE) = memory cell area / total area [%]

- **Energy efficiency (EE)**
  - $\text{TP} / \text{average power} = \text{access / energy [MB/mJ]}$

Single 3D-layer design space

- Cell efficiency vs. max. theoretical throughput (TP) for various banks

(a) 1x 128Mb
(b) 2x 64Mb
(c) 4x 32Mb
(d) 8x 16Mb
Single 3D-layer design space

Energy efficiency (EE) vs. Cell efficiency (CE)

Single 3D-layer ⇒ bank composed of 2x 64Mb tiles independent of technology

Comparison 1Gb

- 1Gb, 8 bank standard 2D-DRAM wo/ IO driver and termination power
- 1Gb stacked eDRAM: extrapolated published 2,39Mb SOI macro [ISSCC]
- 1Gb Mobile Low-Power DDR SDRAM x 16 wo/ IO driver and termination

8x 128Mb = 1Gbit ~10x
Multi-Channel 3D-DRAM Controller

Different request granularities
- But normally fixed to 128 bit (Wide IO JEDEC Standard)

Three types of I/O accesses possible from 32-bit to 128-bit

Front End:
- Synchronization with Dual Clock FIFOs
- Arbitration
- Buffering, Scheduling, Reordering

Back End
- 3D DRAM command Encoding
- Tracking of the BANK status
- Multi IO reconfiguration and data latching for 32/64/128 bit
Fine grained 3D-DRAM access

On the fly switching: 32, 64, 128

Flexible 3D-DRAM system

Single Channel with 128 IO's
Each layer: 4 x 64Mb or 2 x 128Mb
8 layers $\Rightarrow$ 2Gb/channel
Investigated 3D-DRAM Configurations

<table>
<thead>
<tr>
<th>Dens. [Mb]</th>
<th>Architecture</th>
<th># lay. x [org.]</th>
<th># of banks</th>
<th>Techn. [nm]</th>
<th>Cell size [A_{total} [mm²]]</th>
<th>Freq. [MHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDR x128</td>
<td></td>
<td></td>
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<td></td>
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</tr>
<tr>
<td><strong>256</strong></td>
<td>1 x [4x64Mb]</td>
<td>4</td>
<td>58</td>
<td>6F²</td>
<td>16</td>
<td>200</td>
</tr>
<tr>
<td>512</td>
<td>2 x [4x64Mb]</td>
<td>4</td>
<td>58</td>
<td>6F²</td>
<td>26</td>
<td>200</td>
</tr>
<tr>
<td>1024</td>
<td>8 x [2x64Mb]</td>
<td>8</td>
<td>46</td>
<td>6F²</td>
<td>35</td>
<td>300</td>
</tr>
<tr>
<td><strong>2048</strong></td>
<td>8 x [2x128Mb]</td>
<td>8</td>
<td>46</td>
<td>6F²</td>
<td>60</td>
<td>167</td>
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<td>4096</td>
<td>8 x [4x128Mb]</td>
<td>8</td>
<td>45</td>
<td>4F²</td>
<td>97</td>
<td>200</td>
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</tbody>
</table>

**DDR x128**

<table>
<thead>
<tr>
<th>Dens. [Mb]</th>
<th>Architecture</th>
<th># lay. x [org.]</th>
<th># of banks</th>
<th>Techn. [nm]</th>
<th>Cell size [A_{total} [mm²]]</th>
<th>Freq. [MHz]</th>
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<tbody>
<tr>
<td>256</td>
<td>1 x [4x64Mb]</td>
<td>4</td>
<td>58</td>
<td>6F²</td>
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<tr>
<td>512</td>
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<td>58</td>
<td>6F²</td>
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<tr>
<td>1024</td>
<td>8 x [2x64Mb]</td>
<td>8</td>
<td>46</td>
<td>6F²</td>
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<tr>
<td><strong>2048</strong></td>
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<td>46</td>
<td>6F²</td>
<td>69</td>
<td>300</td>
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<tr>
<td>4096</td>
<td>8 x [4x128Mb]</td>
<td>8</td>
<td>45</td>
<td>4F²</td>
<td>98</td>
<td>200</td>
</tr>
</tbody>
</table>

**Density emulates the published Samsung 1Gb WIDE IO chip [15].**

Simulation Set-Up

Emulation of workload via 3 traffic generators:
- Traffic A – Cache misses of a 2 core ARM ~ 100 MB/s per core
- Traffic B – DMA accesses in a SoC (Imaging) ~ 0.8 GB/s
- Traffic C – HD Video DMA accesses ~ 1.5 GB/s
Results with Page hit rate of 50%

The Future - 3D Magali Chip

- 65nm tech, 72mm², 1980 TSVs for 3D NoC, 1250 TSV for wide I/O memory
- Heater, temperature sensors

Source: LETI
Conclusion

- Bandwidth and memory will be big challenges in future computing systems
- We will see new memory devices e.g. memristor based (RRAMs) or spin based memories (MRAMs)
- The future in computation will be 3D
- New heterogeneous memory architectures
- Large opportunity for research