Hardware-Software Contracts for Safe and Secure Systems

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Joint work with
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Andreas Abel, Sebastian Hahn, Valentin Touzeau @ Saarland University

Supported by the European Research Council and an
Intel Strategic Research Alliance (ISRA)

The Need for HW/SW Contracts

"Stone-age" Computing

Applications implemented data transformations:
- e.g. payroll processing

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Hardware:
- isolated, on-site
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IBM System 360/30

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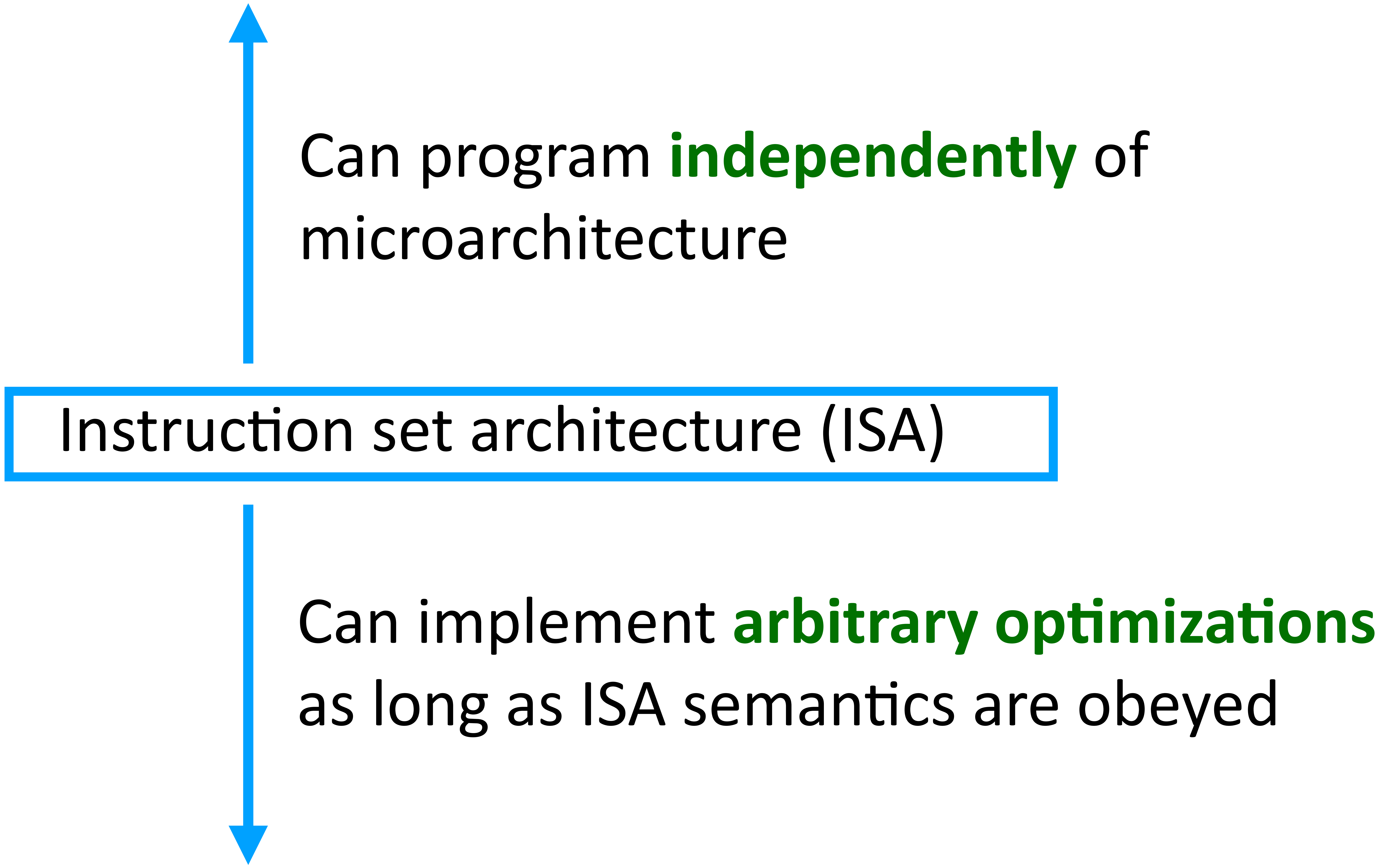
HW/SW Contract: Instruction Set Architecture

ISA Abstraction

$$\begin{tikzcd}
\text{High-level languages} \arrow[d, "\text{Compiler}"] \\
\boxed{\text{Instruction set architecture (ISA)}} \arrow[d, "\text{Implementation}"] \\
\text{Microarchitecture}
\end{tikzcd}$$

ISA Abstraction: Benefits



Can program **independently** of microarchitecture

Instruction set architecture (ISA)

Can implement **arbitrary optimizations** as long as ISA semantics are obeyed

"Modern" (?) Computing

Applications are:

- *Data-driven*: e.g. deep neural networks
- *Distributed*: e.g. locally + in the cloud
- *Open*: e.g. untrusted code in the browser
- *Real-time*: interacting with the physical environment

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What are the implications for HW/SW contracts?

Inadequacy of the ISA + current µArchitectures: Real-time Systems

Instruction set architecture (ISA) **Abstracts from time**

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Instruction set architecture (ISA) **Abstracts from time**

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Can implement arbitrary **unpredictable** optimizations as long as ISA semantics are obeyed

Inadequacy of the ISA + current µArchitectures: Real-time Systems

Programs do not have a **timed semantics**

Programs have **no control** over timing

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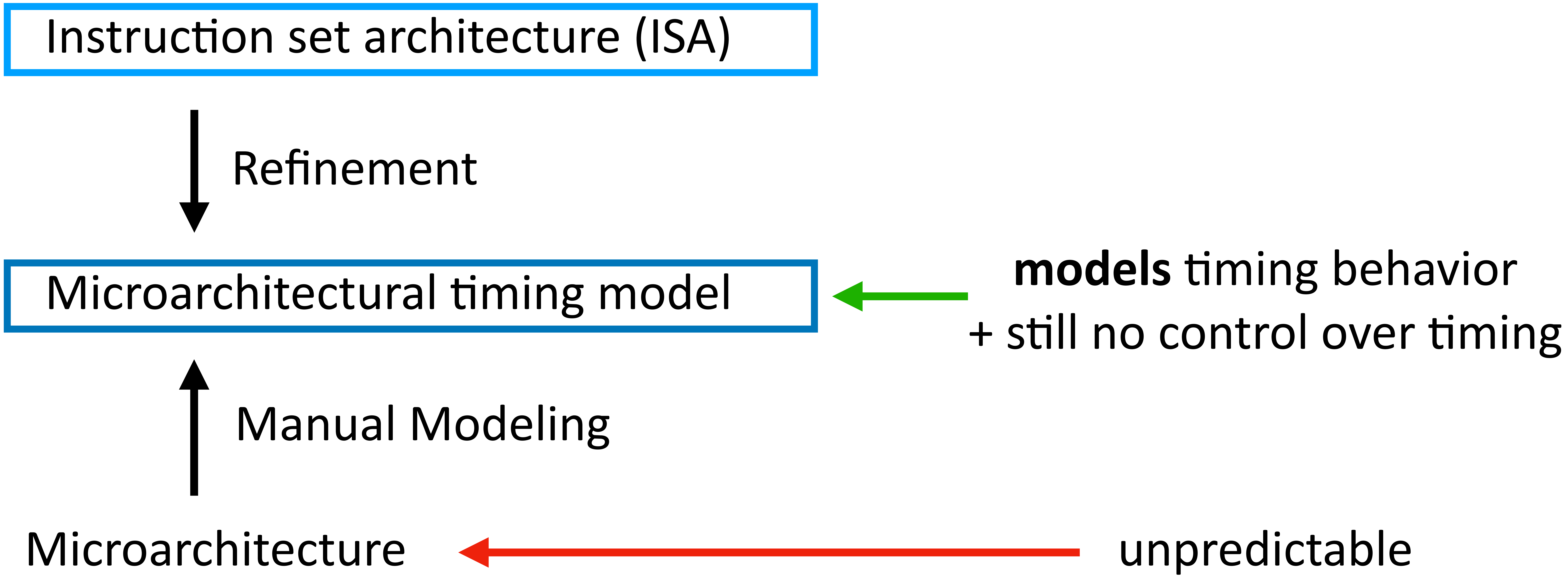
State-of-the-art: Handcrafted Microarchitectural Timing Models


Instruction set architecture (ISA)
Refinement
Microarchitectural timing model
models timing behavior
+ still no control over timing
Manual Modeling
Microarchitecture
unpredictable

State-of-the-art: Handcrafted Microarchitectural Timing Models

Instruction set architecture (ISA)

↓ Refinement

Microarchitectural timing model ← **models** timing behavior
+ still no control over timing

↑ Manual Modeling

Microarchitecture ← unpredictable

Models are
limited to particular microarchitectures
+ probably incorrect
+ yield expensive or imprecise analysis

Wanted: Timed HW/SW Contracts

Timed Instruction Set Architecture

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Timed Instruction Set Architecture

Admit **wide range** of high-performance microarchitectural implementations

Wanted: Timed HW/SW Contracts

Programs have a **timed semantics** that is **efficiently predictable**
Programs have **control** over timing

Timed Instruction Set Architecture

Admit **wide range** of high-performance
microarchitectural implementations

Wanted: Timed HW/SW Contracts

Some answers:

D. Bui, E. Lee, I. Liu, H. Patel, and J. Reineke:
Temporal Isolation on Multiprocessing Architectures
DAC 2011

S. Hahn and J. Reineke:
Design and Analysis of SIC:
A Provably Timing-Predictable Pipelined Processor Core
RTSS 2018

Inadequacy of the ISA + current μArchitectures: Side-channel security

Instruction set architecture (ISA)

No guarantees about side channels

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SPECTRE

Inadequacy of the ISA + current μArchitectures: Side-channel security

Impossible to program securely on top of ISA
- cryptographic algorithms?
- sandboxing untrusted code?

Instruction set architecture (ISA)

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Can implement arbitrary **insecure** optimizations as long as ISA semantics are obeyed

A Way Forward: HW/SW Security Contracts

Hardware-Software Contract = ISA + X

Succinctly captures possible information leakage

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A Way Forward: HW/SW Security Contracts

Can program **securely** on top contract
independently of microarchitecture

Hardware-Software Contract = ISA + X

Succinctly captures
possible information leakage

Can implement **arbitrary** ~~insecure~~ **optimizations**
as long as contract is obeyed

A Concrete Challenge: Spectre

Exploits *speculative execution*

Almost *all* modern *CPUs* are *affected*

Example: Spectre v1 Gadget

```
if (x < A_size)
   y = A[x]
   z = B[y*512]
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1. **x** is out of bounds

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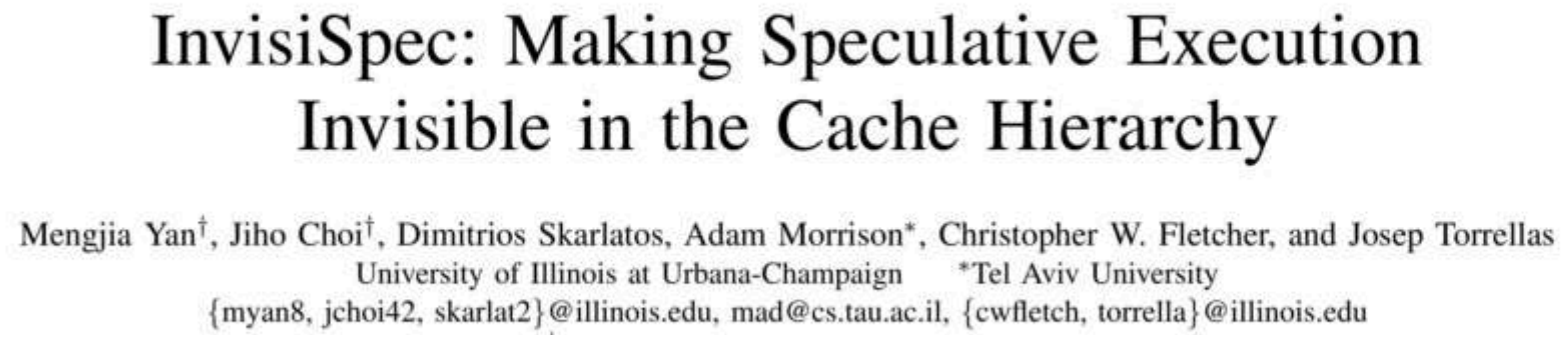
3. Leaks A[x] via data cache

Hardware Countermeasures

Hardware Countermeasures



InvisiSpec: Making Speculative Execution Invisible in the Cache Hierarchy

Mengjia Yan[†], Jiho Choi[†], Dimitrios Skarlatos, Adam Morrison[*], Christopher W. Fletcher, and Josep Torrellas
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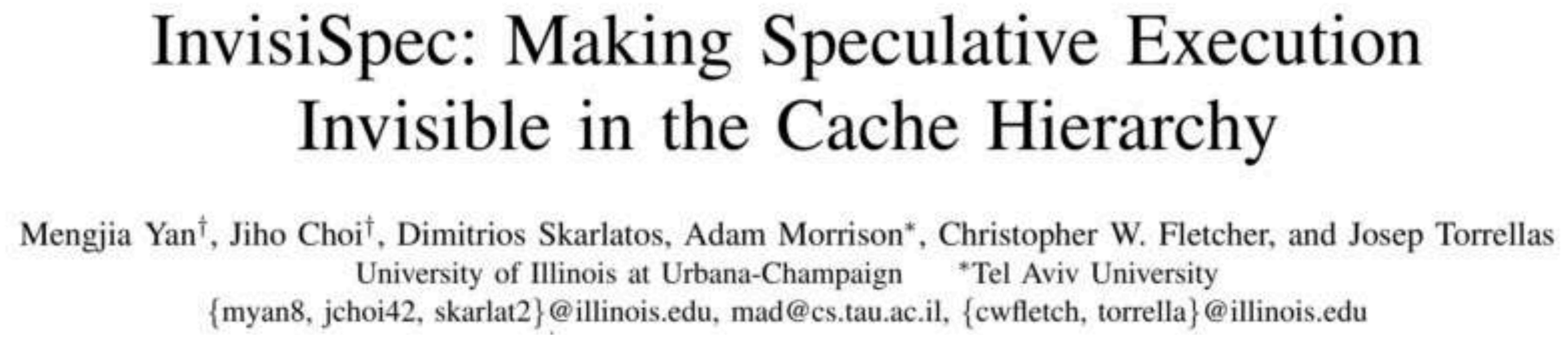
Hardware Countermeasures



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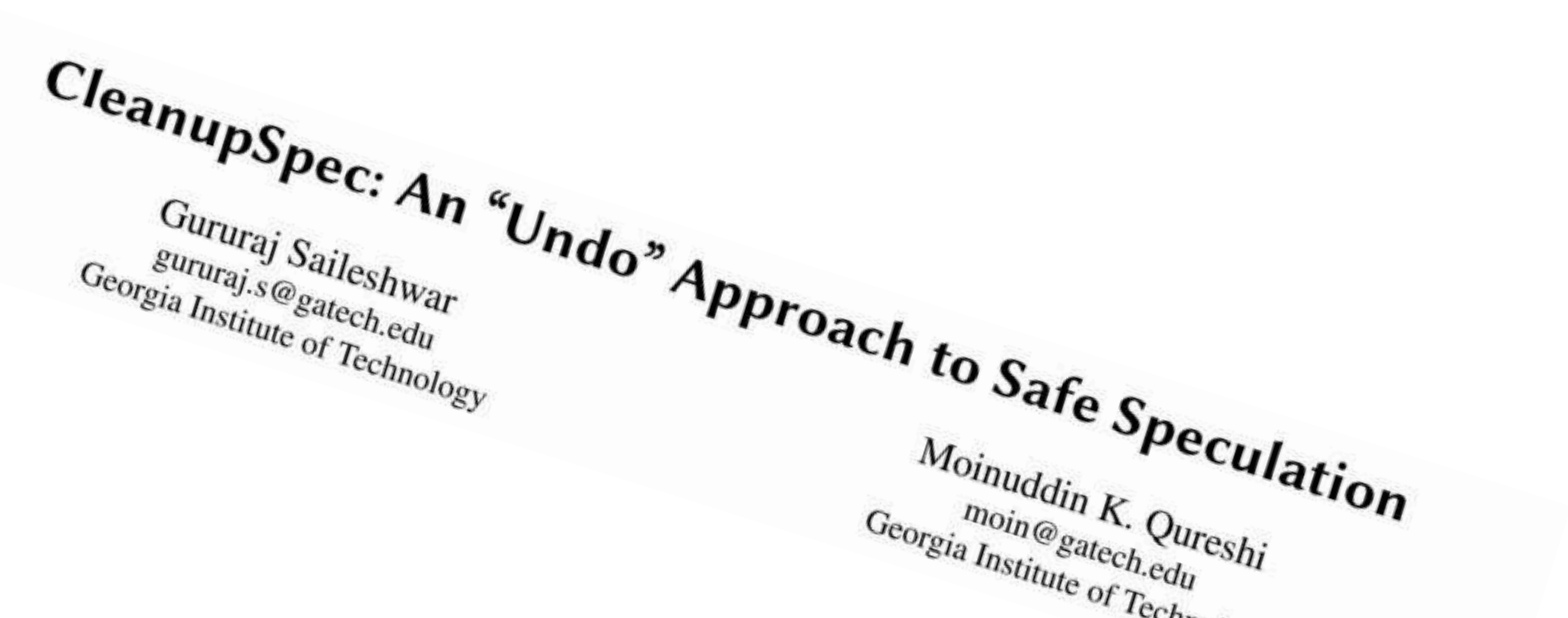

CleanupSpec: An “Undo” Approach to Safe Speculation

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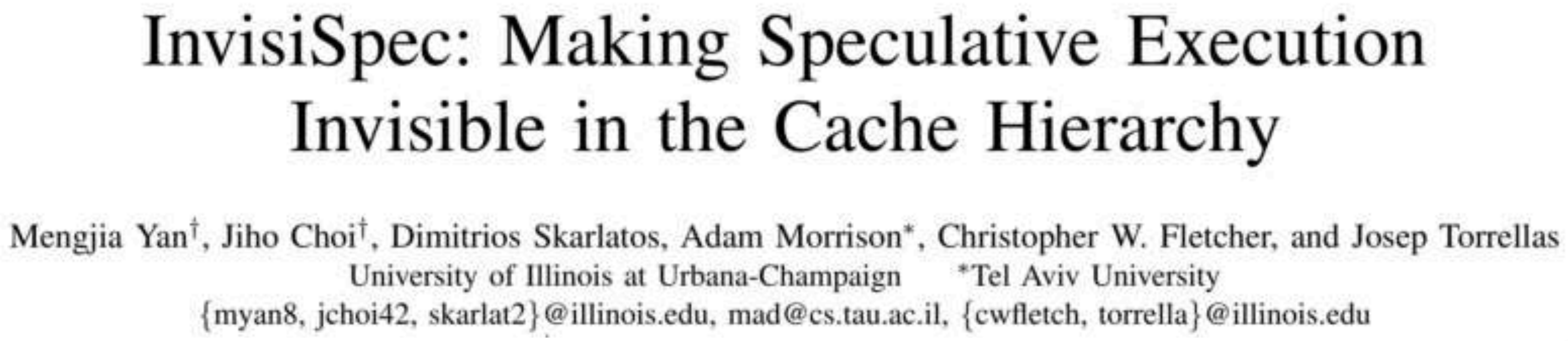
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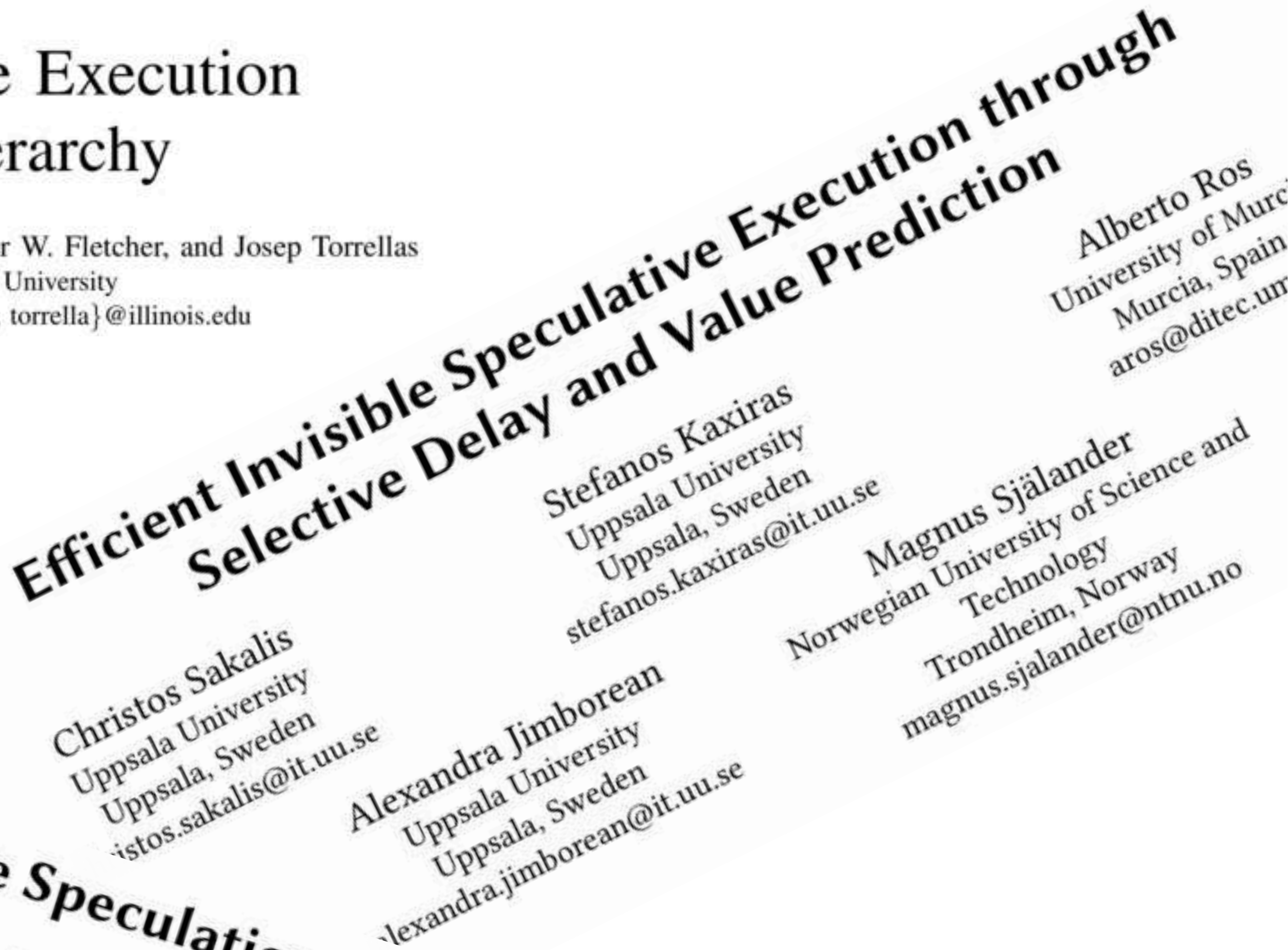
Efficient Invisible Speculative Execution through Selective Delay and Value Prediction

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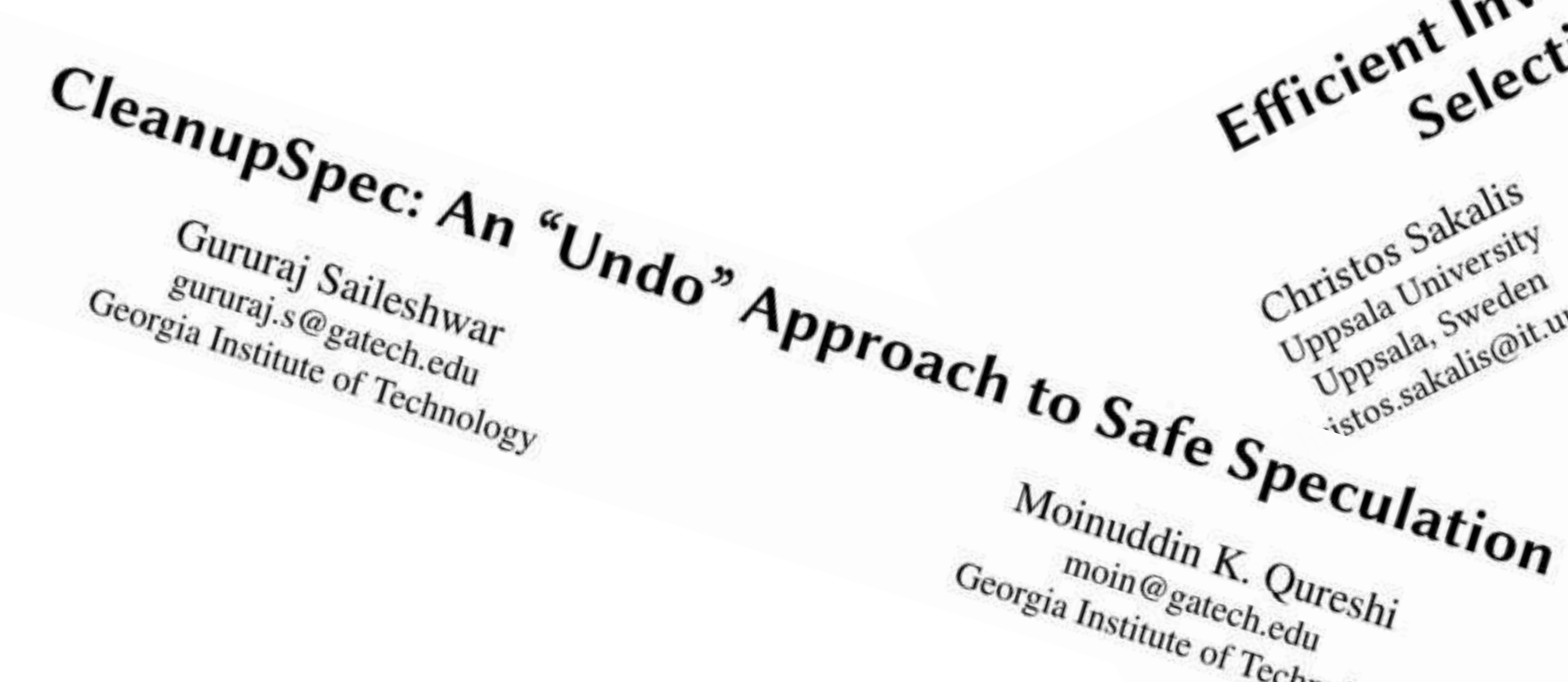
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NDA: Preventing Speculative Execution Attacks at Their Source

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Speculative Taint Tracking (STT): A Comprehensive Protection for Speculatively Accessed Data

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Delay loads until they can be retired
[Sakalis et al., ISCA'19]

Delay loads until they cannot be squashed
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[STT and NDA, MICRO’19]

What security properties do HW countermeasures enforce?

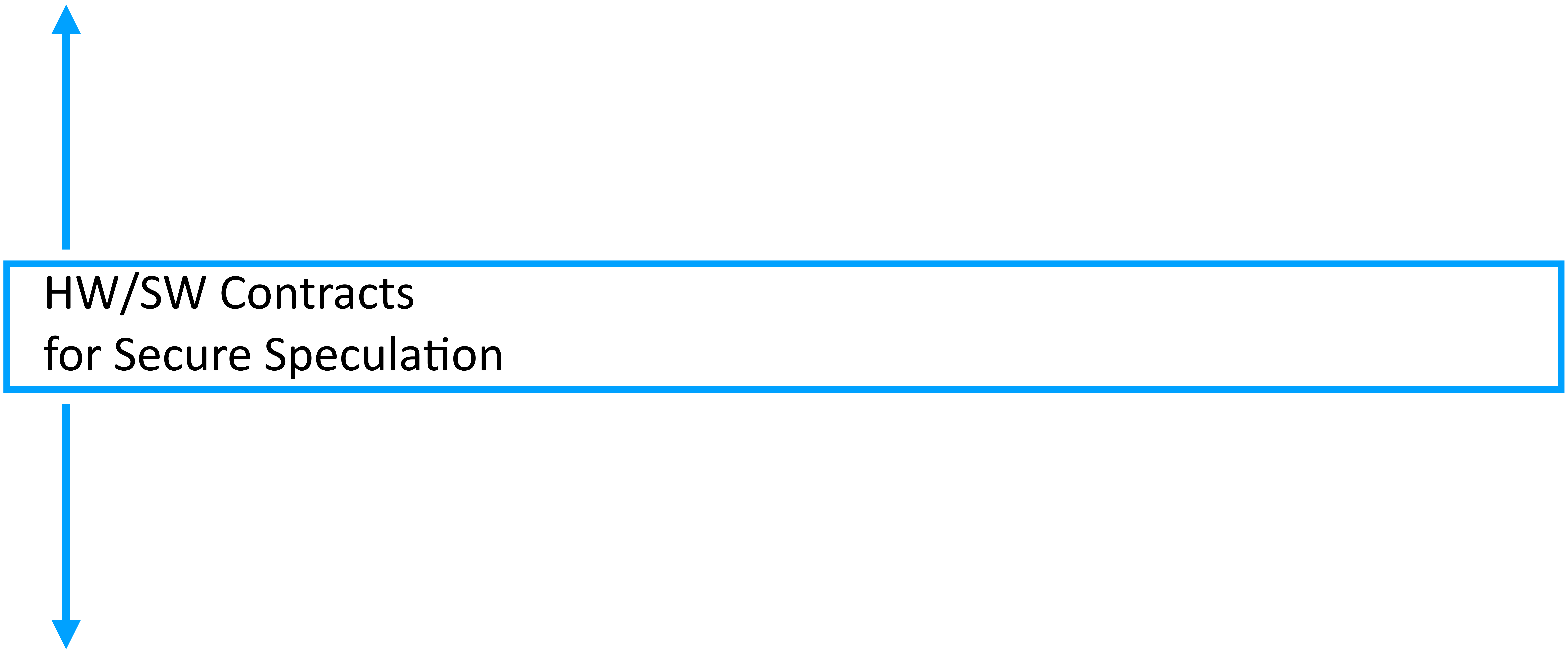
How can we program securely?

A Proof of Concept

M. Guarnieri, B. Köpf, J. Reineke, and P. Vila
Hardware-Software Contracts for Secure Speculation
S&P (Oakland) 2021

Hardware-Software Contracts

HW/SW Contracts for Secure Speculation



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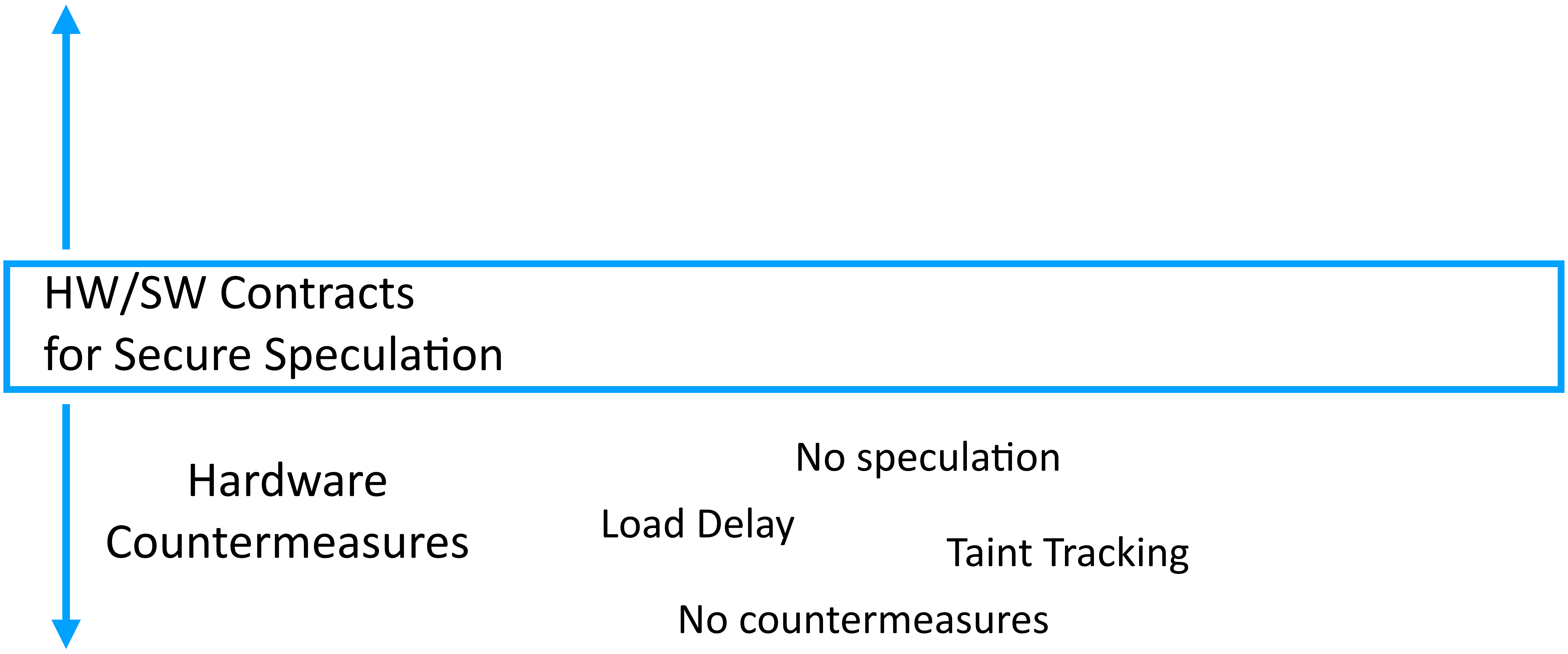
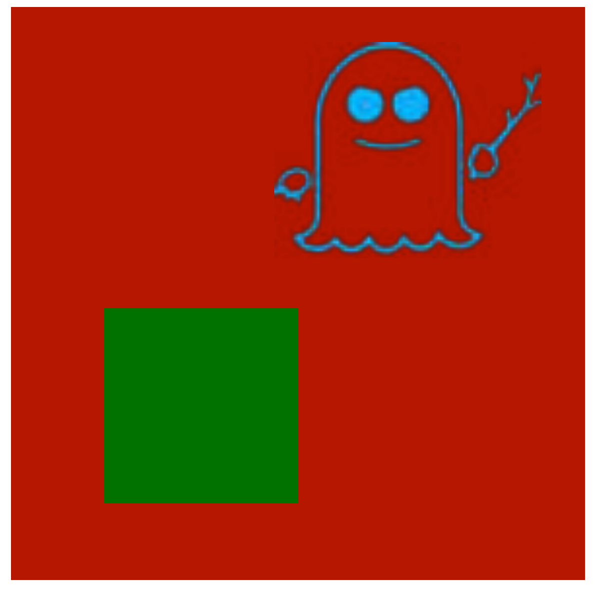
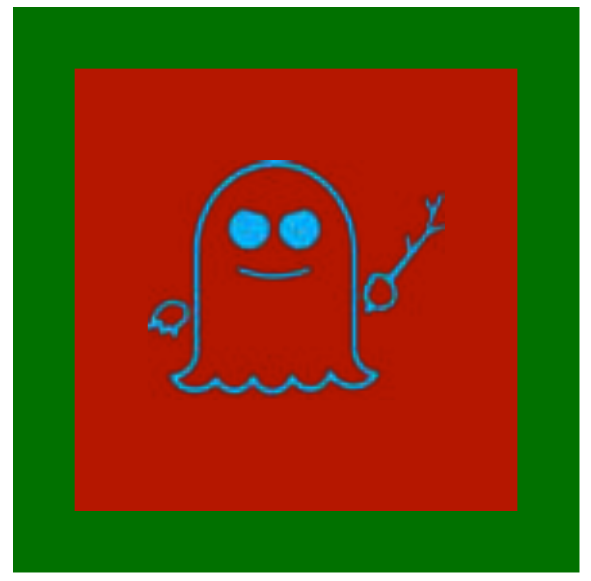


HW/SW Contracts for Secure Speculation

Secure Programming



Constant-time



Sandboxing

HW/SW Contracts for Secure Speculation

Hardware Countermeasures

No speculation

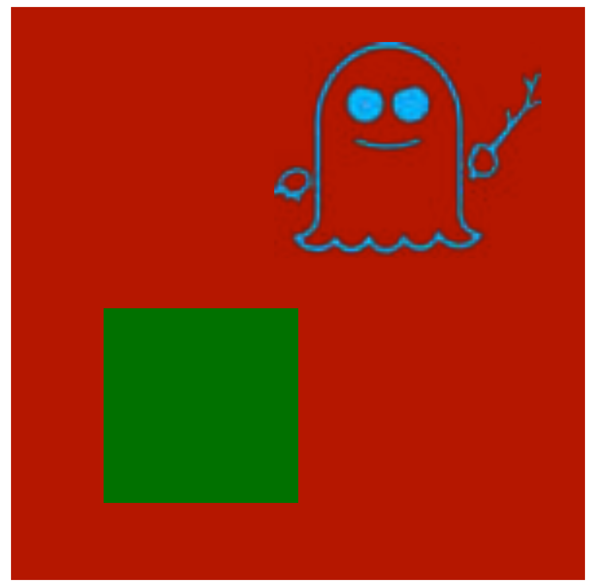
Load Delay

Taint Tracking

No countermeasures

HW/SW Contracts for Secure Speculation

Secure Programming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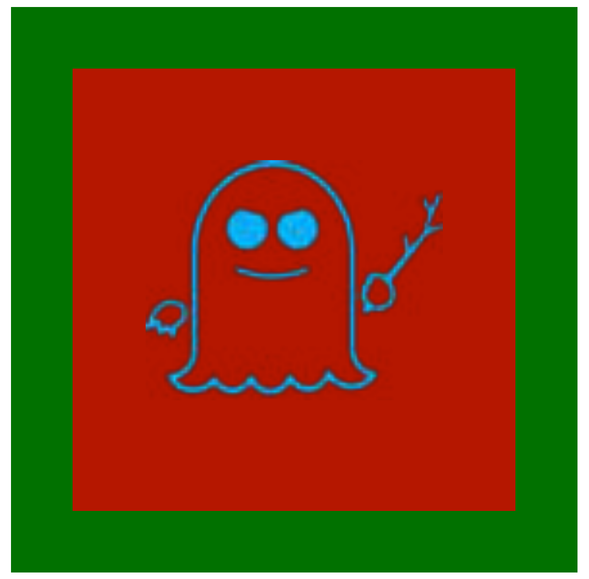
Sandboxing

HW/SW Contracts for Secure Speculation

Desiderata: simple mechanism-independent precise

Hardware Countermeasures

No speculation

Load Delay

Taint Tracking

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Ingredients of a Formalization

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Instruction Set Architecture

Arch. states: σ

Arch. semantics: $\sigma \rightsquigarrow \sigma'$

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Microarchitecture

Hardware states: $\langle \sigma, \mu \rangle$

Hardware semantics: $\langle \sigma, \mu \rangle \Rightarrow \langle \sigma', \mu' \rangle$

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Microarchitecture

Hardware states: $\langle \sigma, \mu \rangle$

Hardware semantics: $\langle \sigma, \mu \rangle \Rightarrow \langle \sigma', \mu' \rangle$

Adversary model

µArch traces: $\{\!|\, p \,|\!\}(\sigma) = \mu_0\mu_1 \ldots \mu_n$

Contracts

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A deterministic, labelled semantics $\xrightarrow{\tau}$ for the ISA

Contracts

Observations expose security-relevant *μArch events*

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Observations expose security-relevant *μArch events*

Contract

A deterministic, labelled semantics $\boxed{\xrightarrow{\tau}}$ for the ISA

Contract traces: $[\![p]\!](\sigma) = \tau_1\tau_2\ldots\tau_n$

Contract satisfaction

Hardware $\{\!|\cdot|\!\}$ satisfies contract $[\![\cdot]\!]$ if for all programs p and arch. states σ, σ': if $[\![p]\!](\sigma) = [\![p]\!](\sigma')$ then $\{\!|p|\!\}(\sigma) = \{\!|p|\!\}(\sigma')$

Contracts for Secure Speculation

Contracts for Secure Speculation

Contract =

Execution Mode · Observer Mode

Contracts for Secure Speculation

Contract =

$\boxed{\text{Execution Mode}} \cdot \text{Observer Mode}$

How are programs executed?

Contracts for Secure Speculation

Contract =

Execution Mode · $\boxed{\text{Observer Mode}}$

How are programs executed?

What is visible about the execution?

Contracts for Secure Speculation

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$\boxed{\text{Execution Mode}} \cdot \text{Observer Mode}$

Contracts for Secure Speculation

Contract =

$\boxed{\text{Execution Mode}}$ · Observer Mode

seq — sequential execution

spec — mispredict branch instructions

Contracts for Secure Speculation

Contract =

Execution Mode · $\boxed{\text{Observer Mode}}$

Contracts for Secure Speculation

Contract =

Execution Mode · $\boxed{\text{Observer Mode}}$

pc — only program counter

ct — **pc** + addr. of loads and stores

arch — **ct** + loaded values

A Lattice of Contracts

$$\begin{tikzcd}
 & & \textbf{seq-ct} \arrow[r] & \top \\
 & \textbf{seq-arch} \arrow[ur] & \textbf{seq-ct+spec-pc} \arrow[u] & \\
\bot \arrow[r] & \textbf{spec-arch} \arrow[u] \arrow[r] & \textbf{spec-ct} \arrow[u] &
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\text{Leaks “everything”} \arrow[u, bend left] & & &
\end{tikzcd}$$

A Lattice of Contracts

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Leaks addresses of non-spec. loads/stores/ instruction fetches

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A Lattice of Contracts

Leaks "nothing"

Leaks all data accessed non-speculatively

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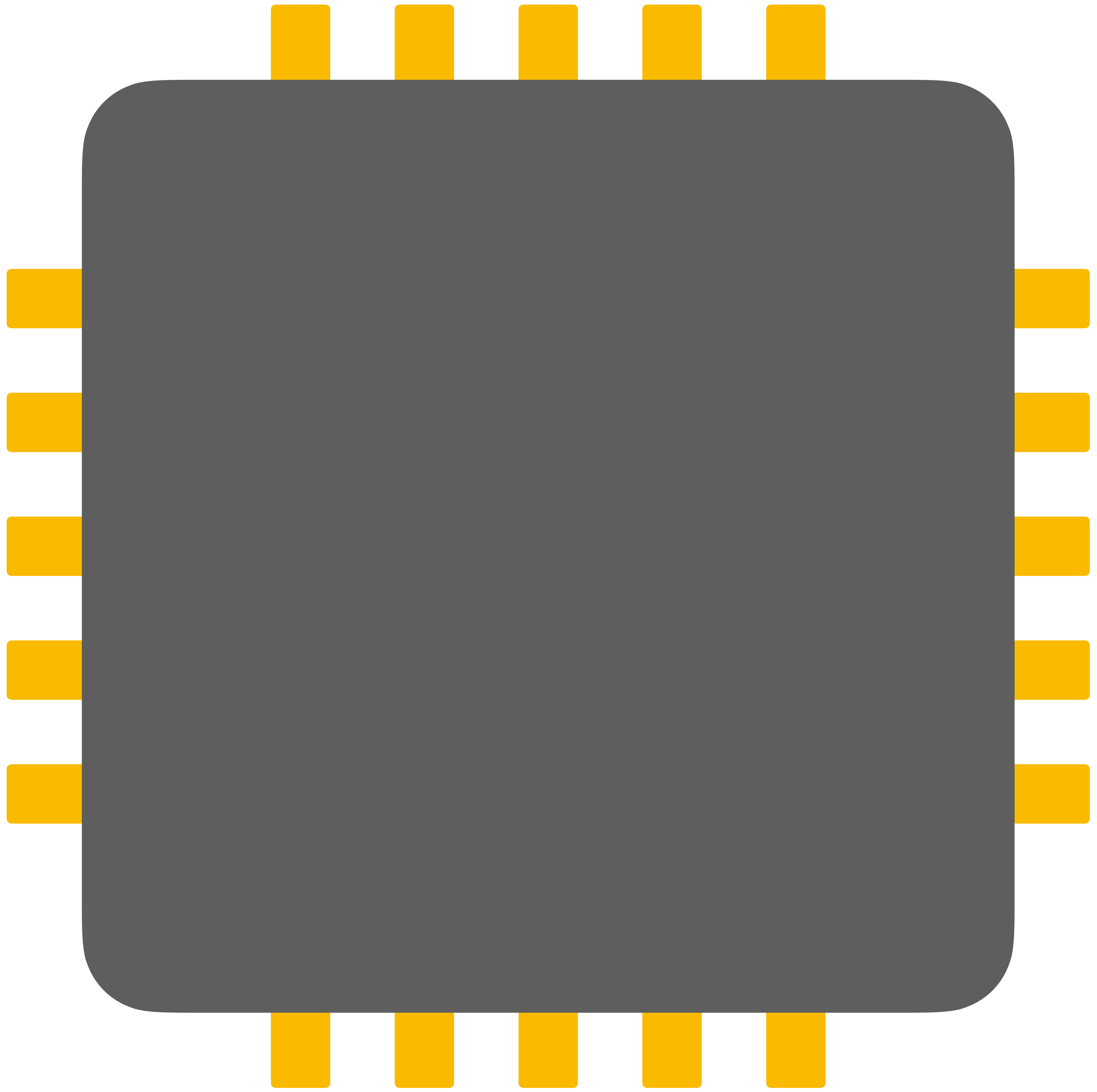
Hardware Countermeasures

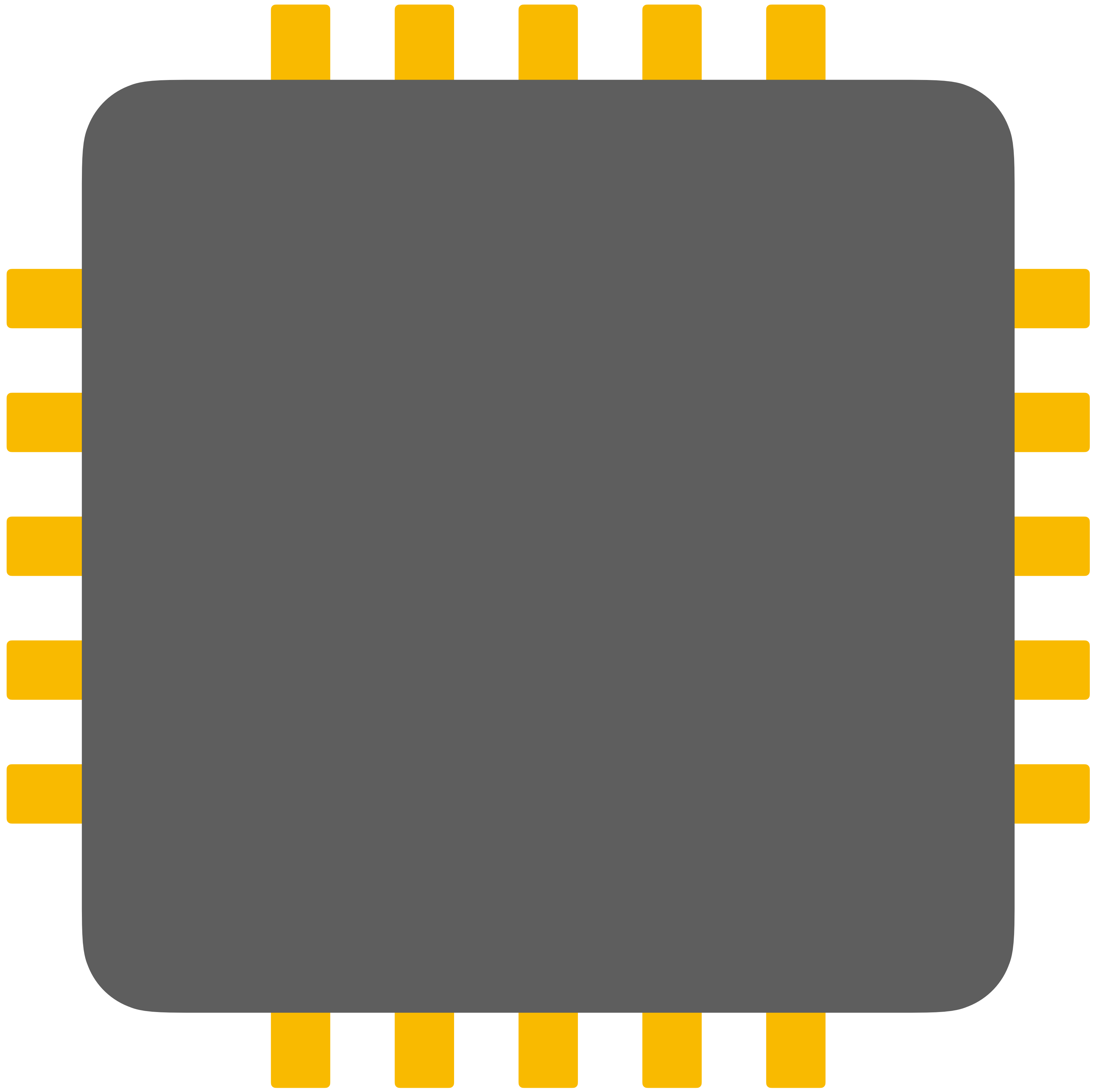
A Simple Processor



A Simple Processor

3-stage pipeline

(fetch, execute, retire)



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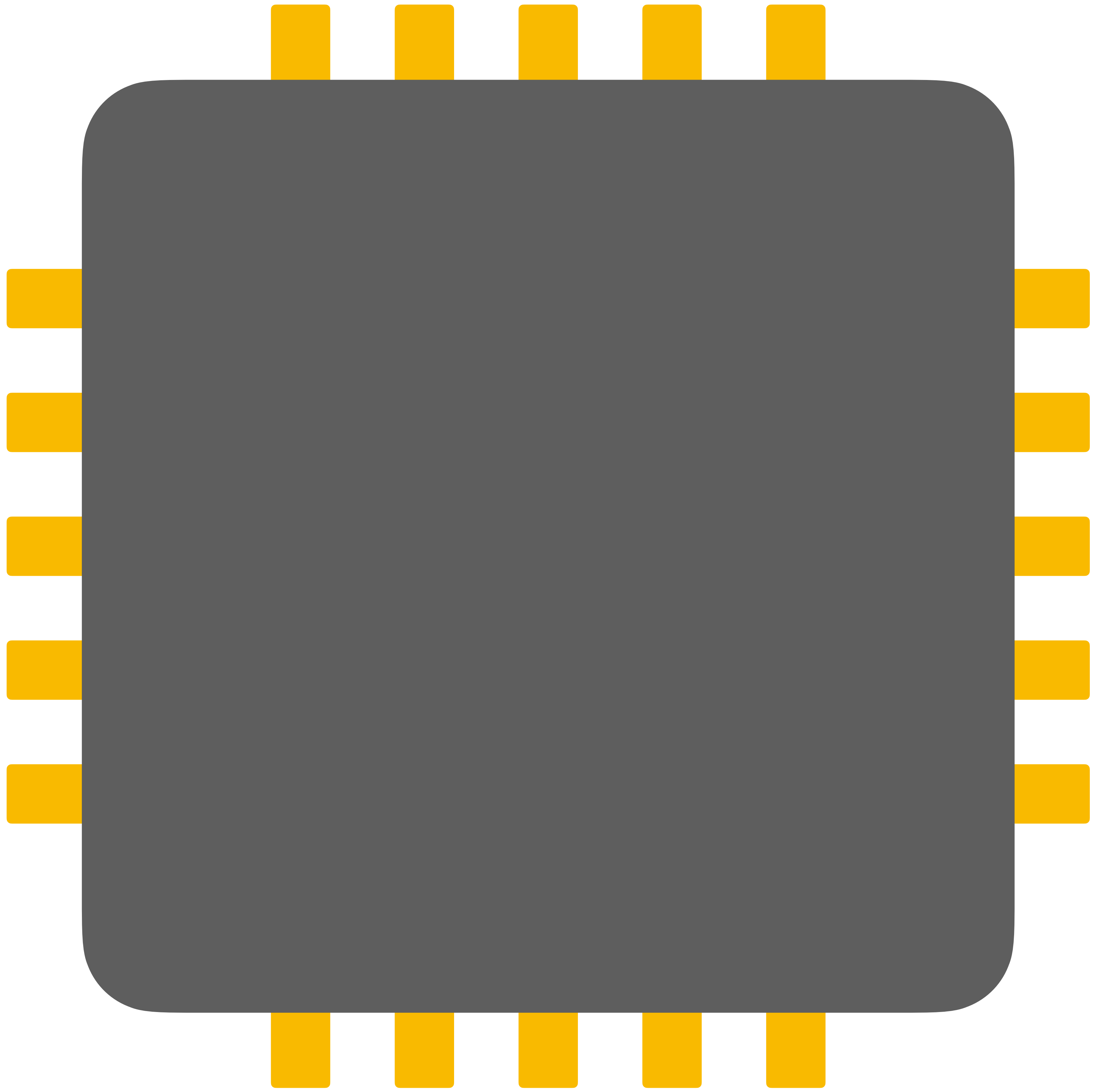

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Speculative and *out-of-order* execution

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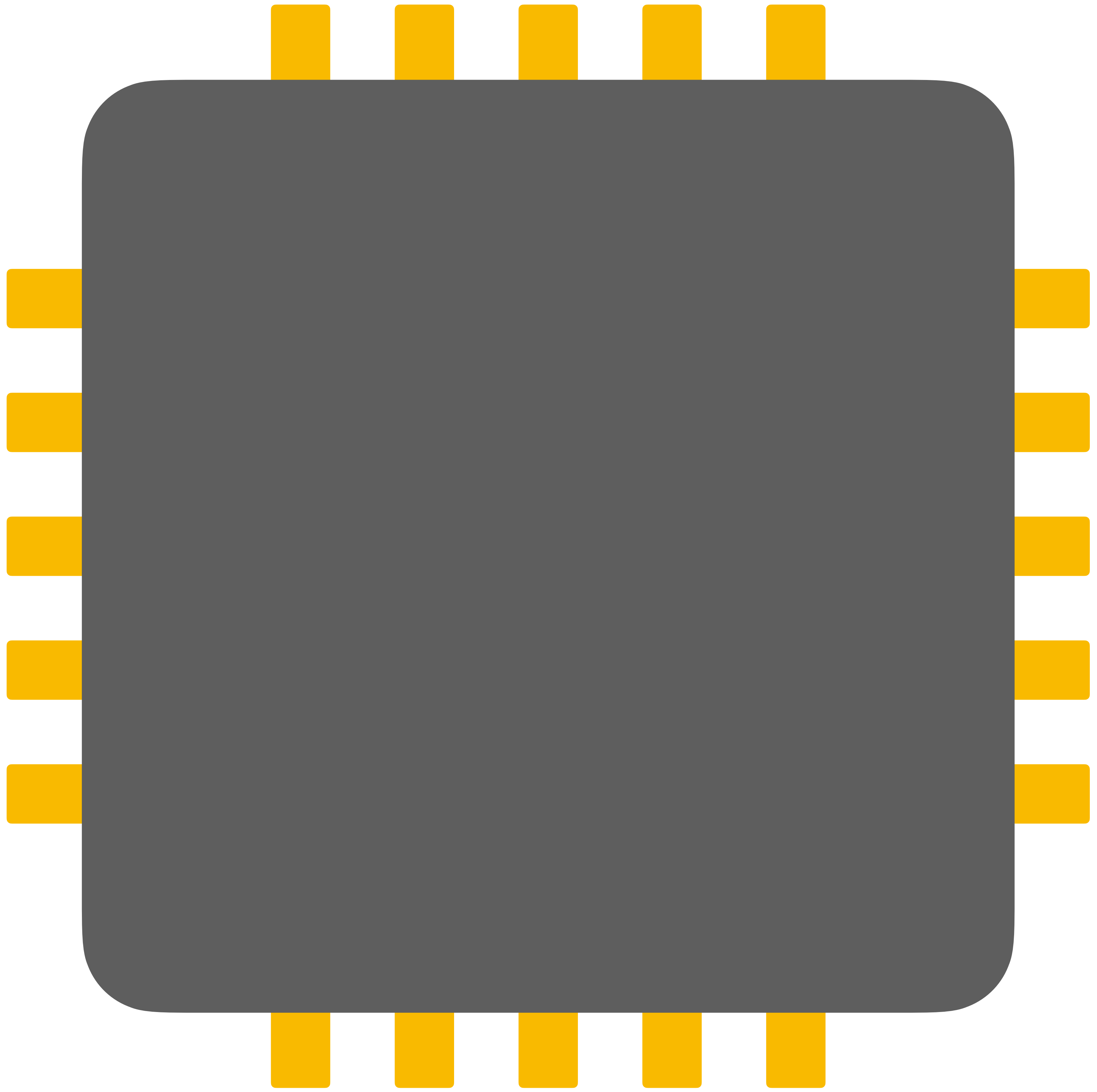

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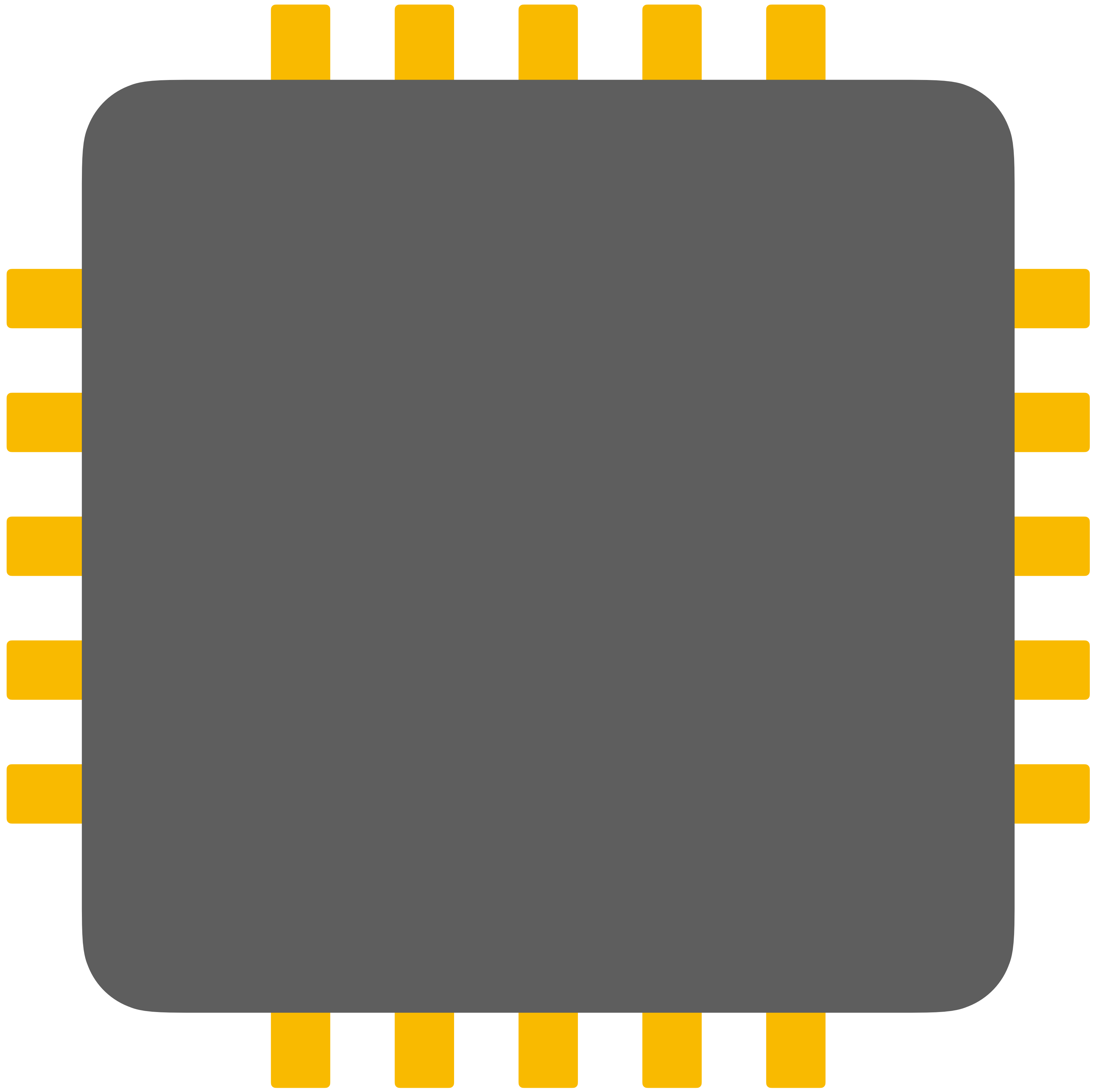

3-stage pipeline
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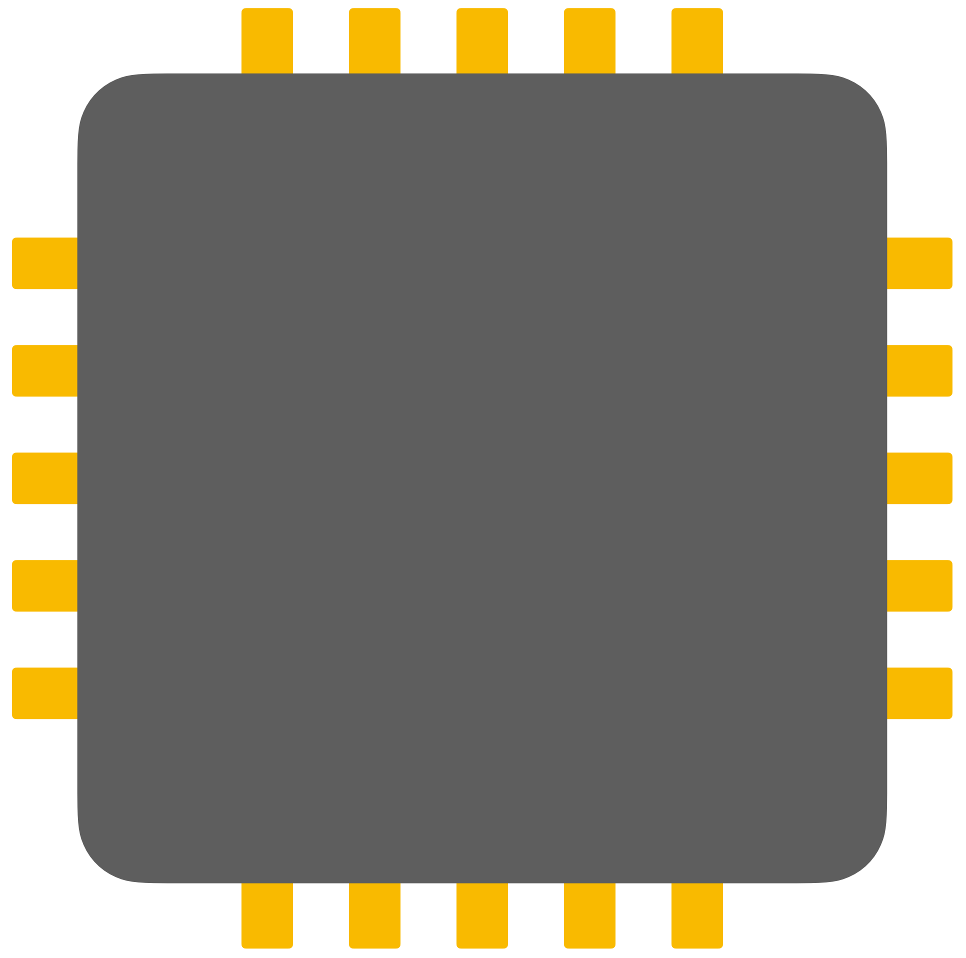
Speculative and *out-of-order* execution

Parametric in *branch predictor* and *memory hierarchy*

Different *schedulers* for different countermeasures

Disabling Speculative Execution



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Satisfies **seq-ct**

Eager Load Delay *[Sakalis et al., ISCA’19]*

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Delaying loads until all sources of *speculation are resolved*

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Security guarantees?

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`B[z]` delayed until `x < A_size` is resolved

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➡ Also satisfies **seq-arch**

No Countermeasures *[The World until 2018]*

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Security Guarantees

$$\begin{tikzcd}
 & \text{seq-ct} \\
\text{seq-arch} \arrow[ur] & \text{seq-ct+spec-pc} \arrow[u] \\
 & \text{spec-ct} \arrow[u] \\
\text{spec-arch} \arrow[uu] \arrow[ur] &
\end{tikzcd}$$

Security Guarantees

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Secure Programming

Secure Programming: Foundations

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Program p is ***non-interferent*** wrt contract $[\![\cdot]\!]$ and policy π if for all arch. states σ, σ': if $\sigma \approx_\pi \sigma'$ then $[\![p]\!](\sigma) = [\![p]\!](\sigma')$

Secure Programming: Foundations

Specify secret data

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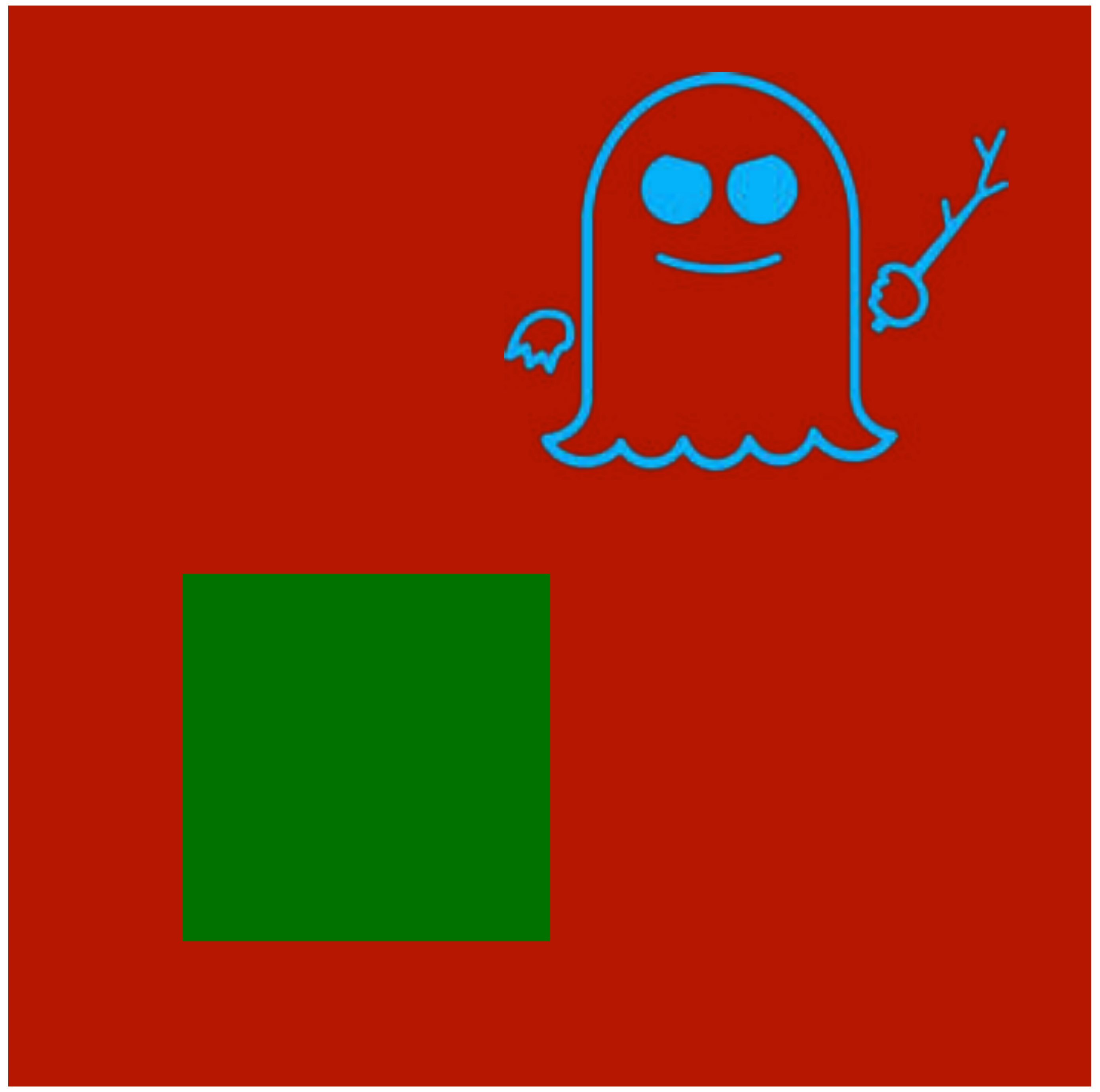
Theorem

If p is ***non-interferent*** wrt contract $[\![\cdot]\!]$ and policy π,

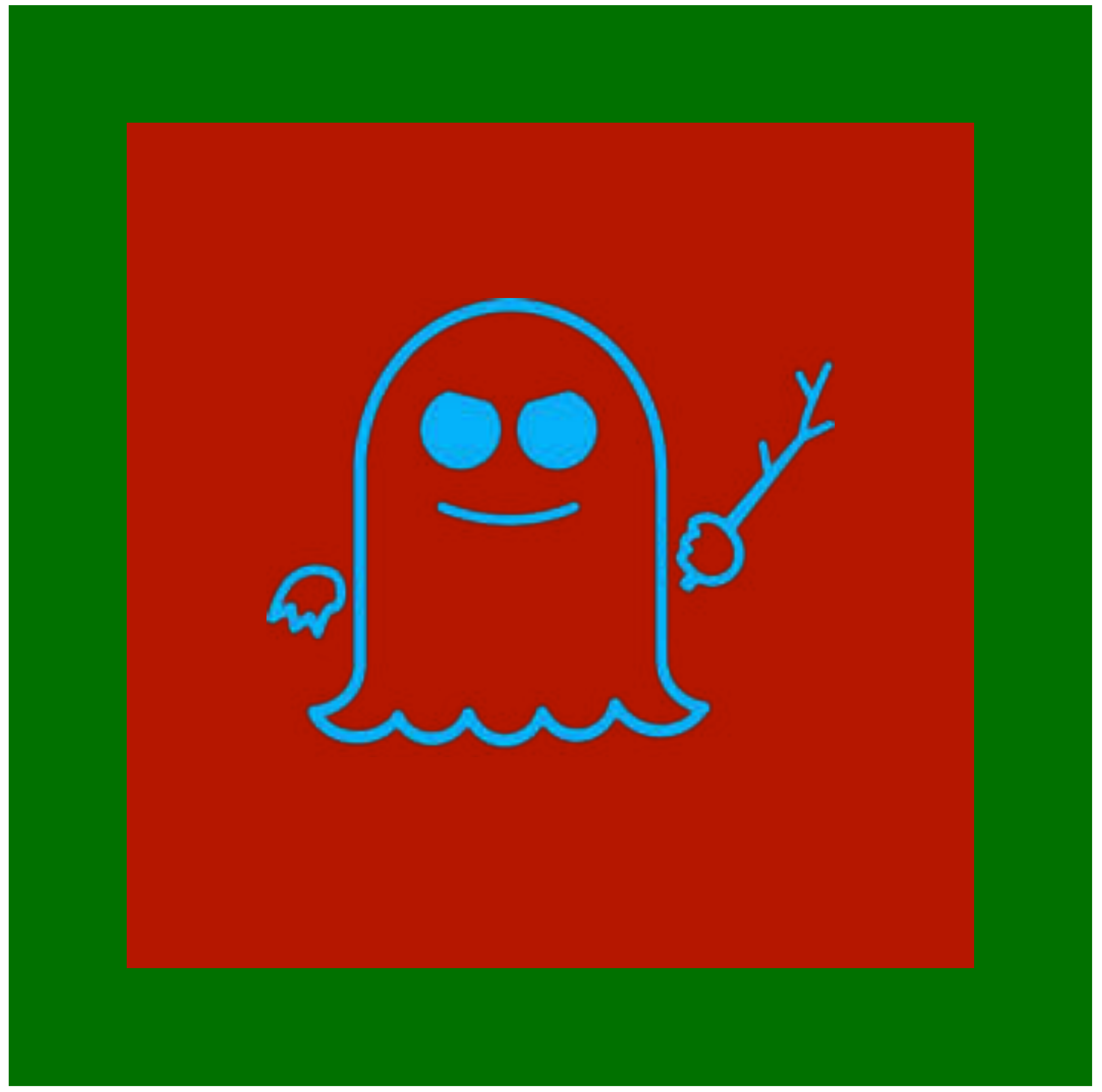
and hardware $\{\!|\cdot|\!\}$ satisfies $[\![\cdot]\!]$, then

p is ***non-interferent*** wrt hardware $\{\!|\cdot|\!\}$ and policy π

Two Flavors of Secure Programming



Constant-time



Sandboxing

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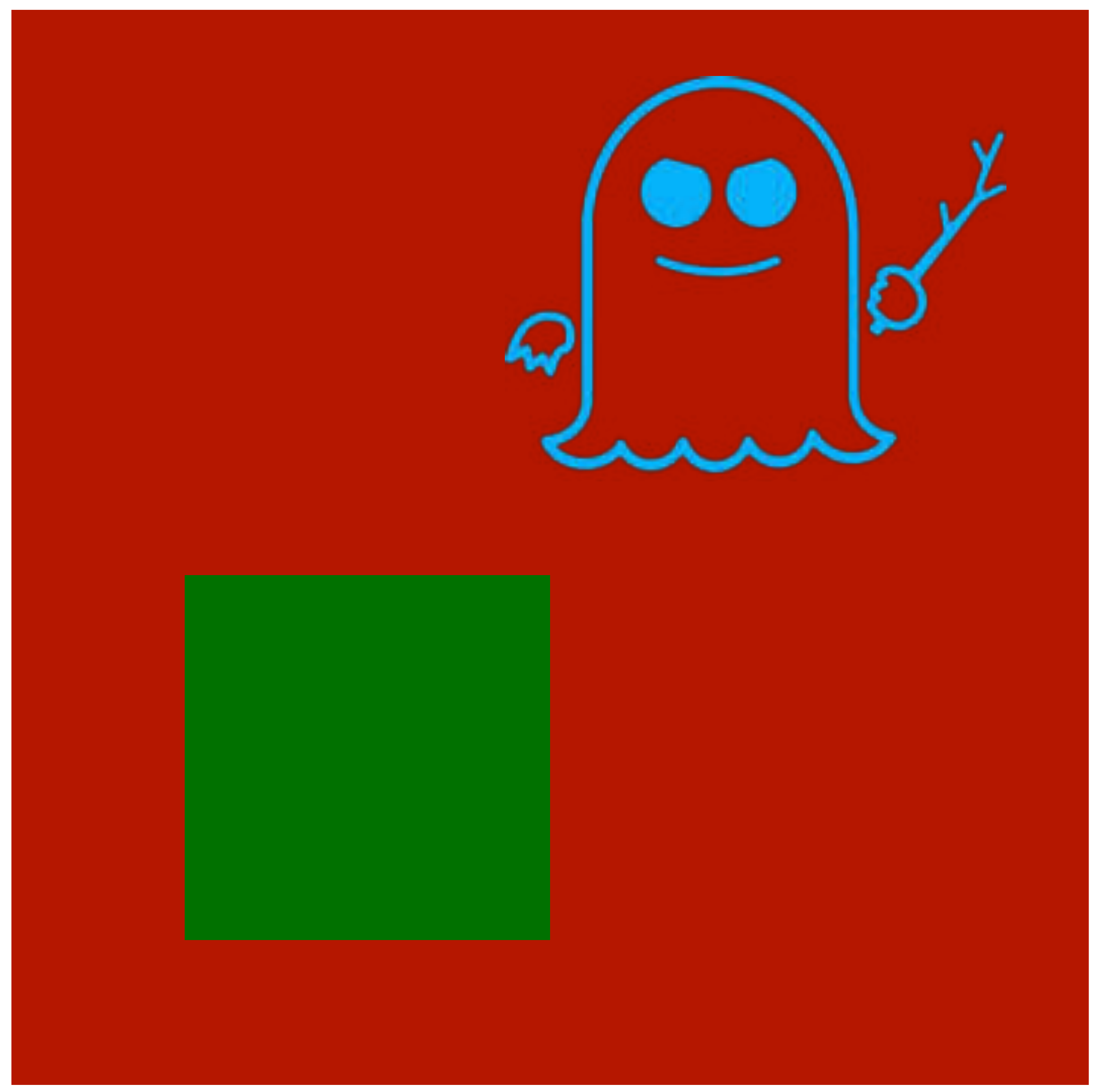

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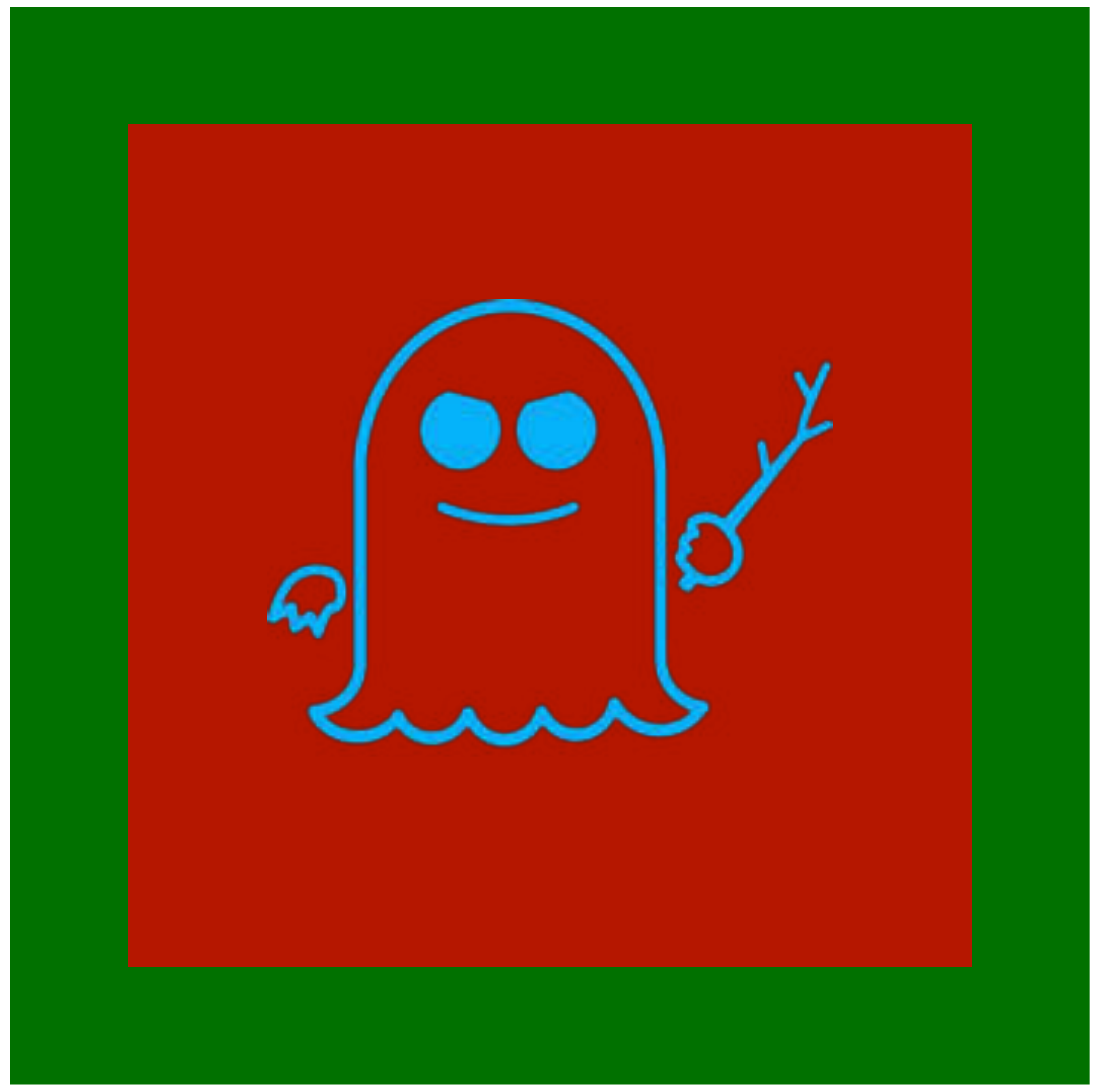

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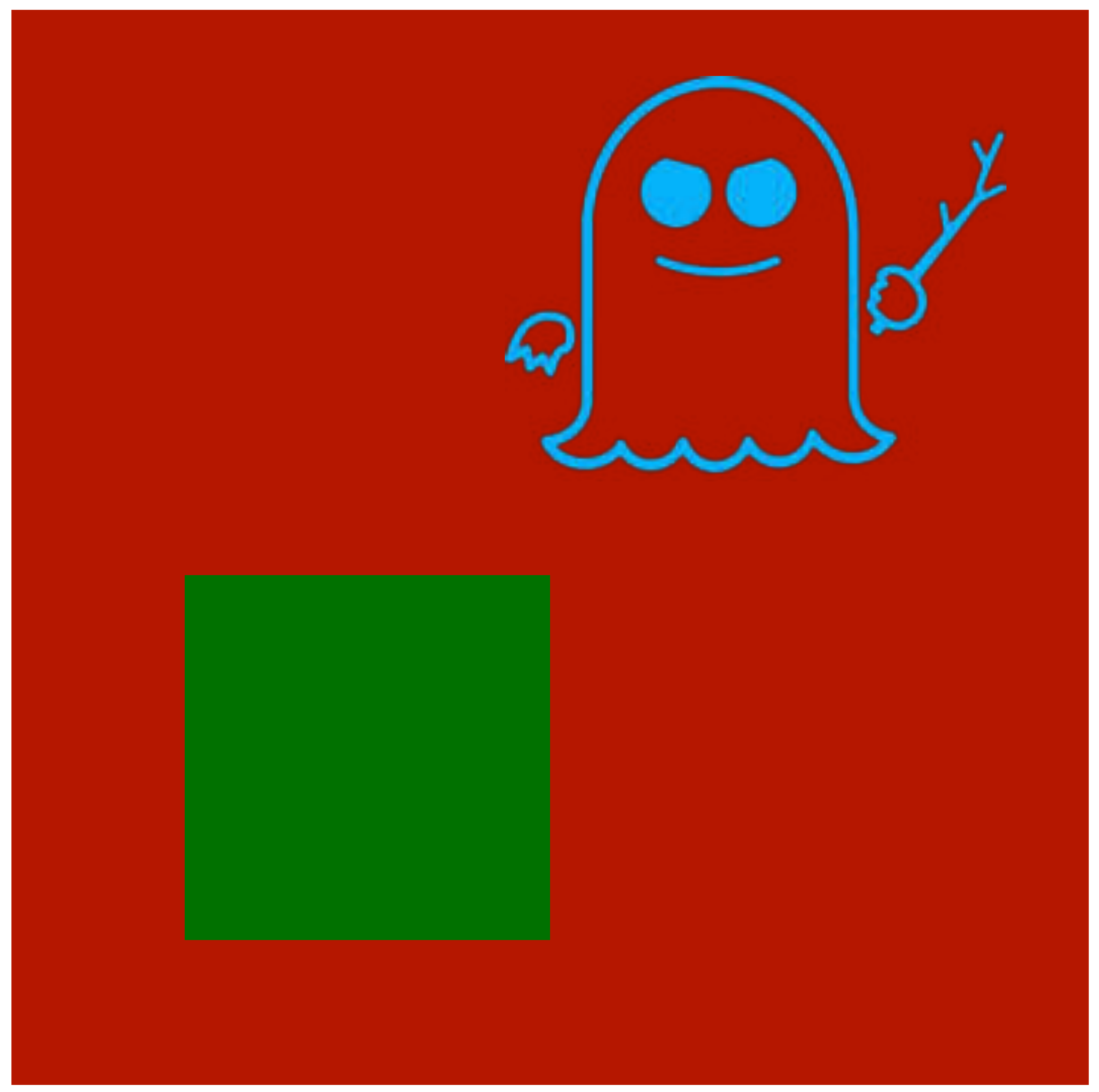

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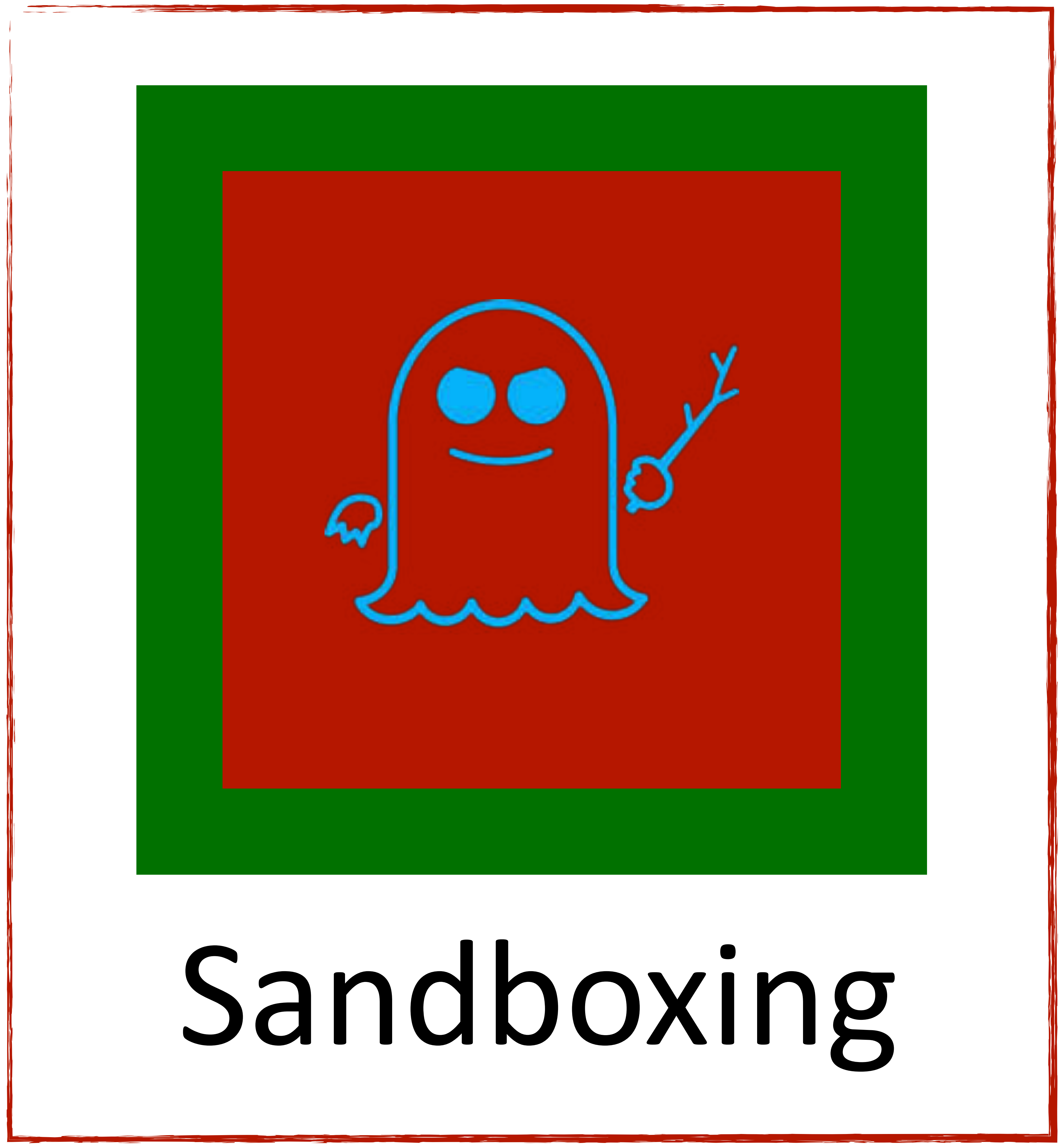

Sandboxing

Constant-time Programming

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Traditional CT wrt policy $\pi \equiv$ non-interference wrt **seq-ct** and π

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Control-flow and memory accesses do not depend on secrets

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Constant-time Programming

Control-flow and memory accesses do not depend on secrets

Traditional CT wrt policy π $\equiv$ non-interference wrt **seq-ct** and π

General CT wrt π and $[\![\cdot]\!]$ $\equiv$ non-interference wrt $[\![\cdot]\!]$ and π

Sandboxing

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Traditional SB wrt policy $\pi \equiv$ non-interference wrt **seq-arch** and π

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Programs never access high memory locations (out-of-sandbox)

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General SB wrt π and $[\![\cdot]\!]$ $\equiv$

Traditional SB wrt π + non-interference wrt π and $[\![\cdot]\!]$

Checking Secure Programming

	Constant-time
seq-ct	Traditional constant-time (= non-interference wrt **seq-ct**)
seq-arch	Non-interference wrt **seq-arch**
spec-ct	… + Spec. non-interference *[Spectector, S&P'20]*

Checking Secure Programming

	Constant-time
seq-ct	Traditional constant-time (= non-interference wrt **seq-ct**)
seq-arch	Non-interference wrt **seq-arch** ⚡
spec-ct	… + Spec. non-interference *[Spectector, S&P'20]*

Checking Secure Programming

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seq-ct	Traditional sandboxing (= non-interference wrt **seq-arch**)
seq-arch	Traditional sandboxing
spec-ct	… + weak SNI

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Conclusions

Need to rethink **hardware-software contracts** with security and safety in mind!

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Should strive for **simple** and **mechanism-independent** contracts.

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Find out more in our paper:

M. Guarnieri, B. Köpf, J. Reineke, and P. Vila
Hardware–Software Contracts for Secure Speculation
S&P (Oakland) 2021