Institute of Microelectronic Systems

Hearing 4all

Leibniz Universität Hannover

Design of Low Power Hearing Aid Processors

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Contents

- Hearing loss and modern hearing aids
- Concept of an Application Specific Instruction-Set Processor
- How to improve hearing aids with ASIPs
- The KAVUAKA ASIP architecture
- Current trends in hearing aid processor design
- Conclusion

Nicht sehen können trennt von den Dingen, nicht hören können von den Menschen.

Immanuel Kant

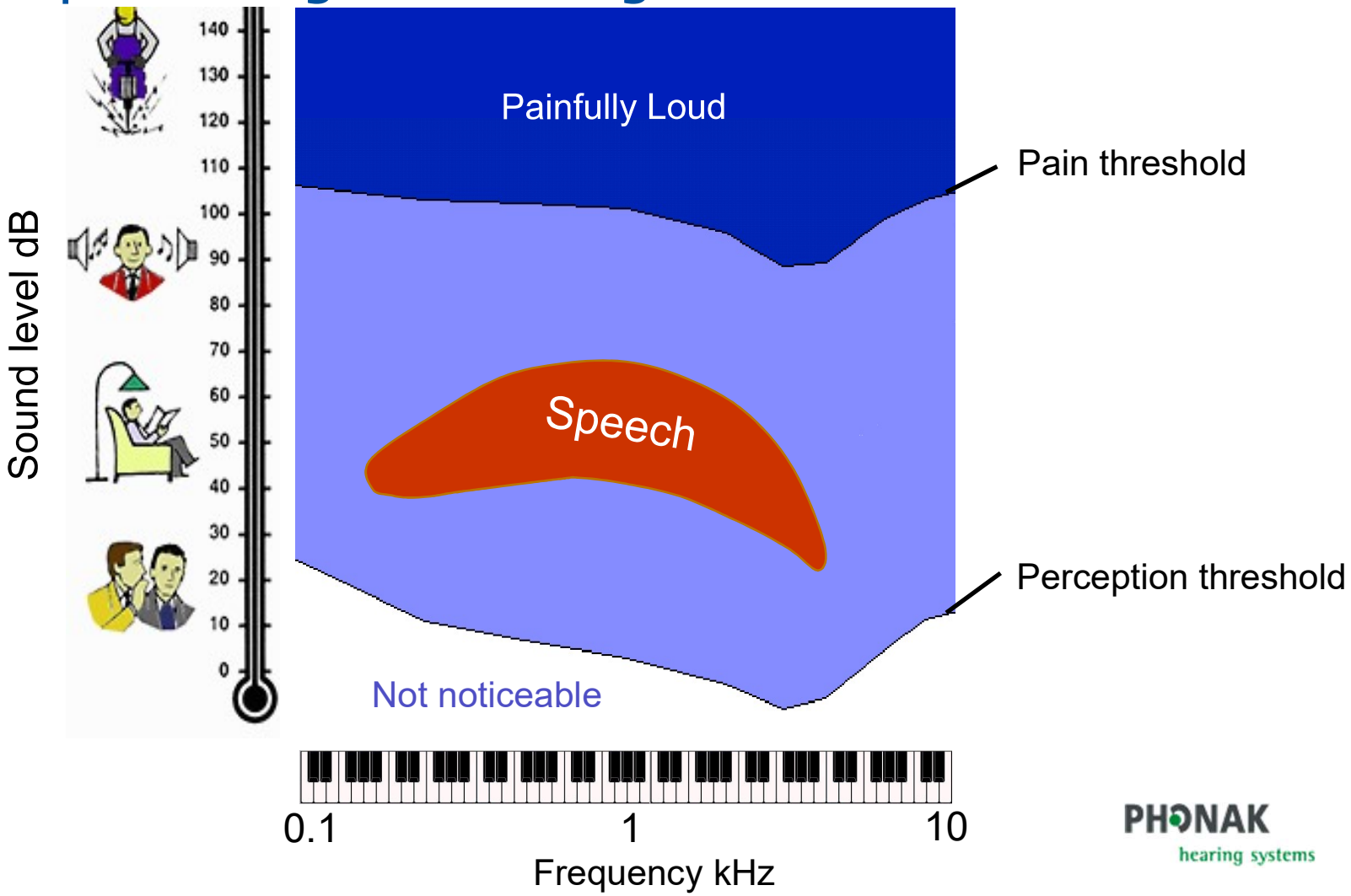
Quelle: wikimedia.org

Hearing Loss in modern Society

- Social interaction is based on communication
- Hearing loss is one of the most common sensoric deficits and often unknown or untreated

"https://www.preciosahome.com/buddha-bar/ "

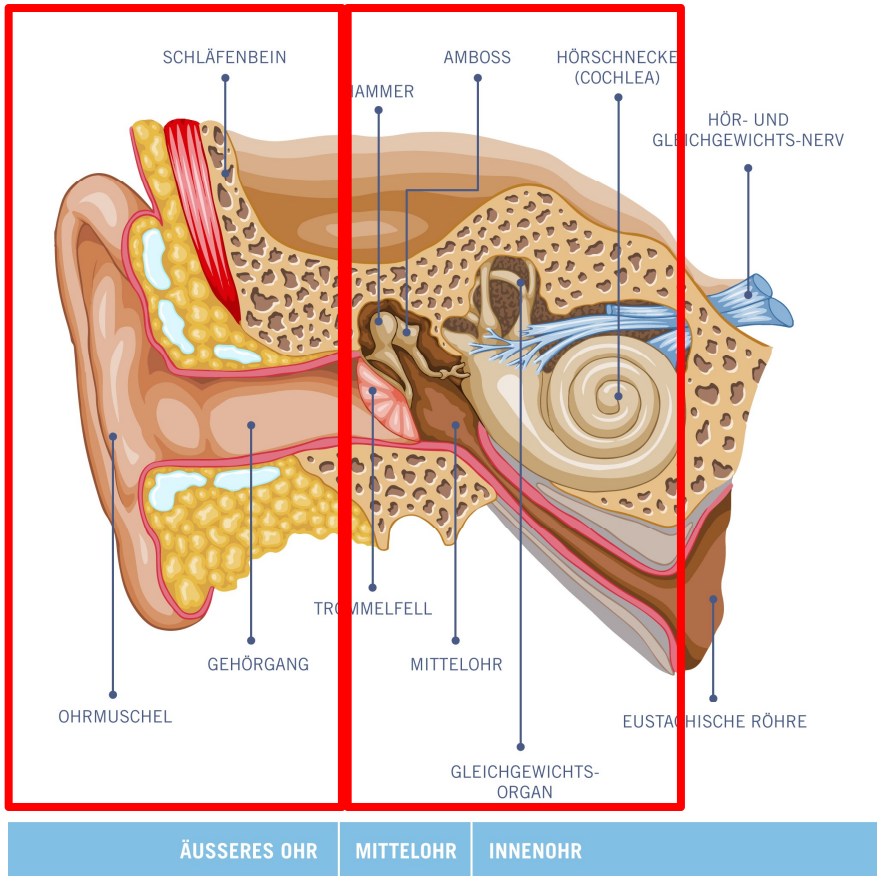
Perceptual Range of Hearing



PHONAK hearing systems

Hearing Loss in the Outer and Middle Ear

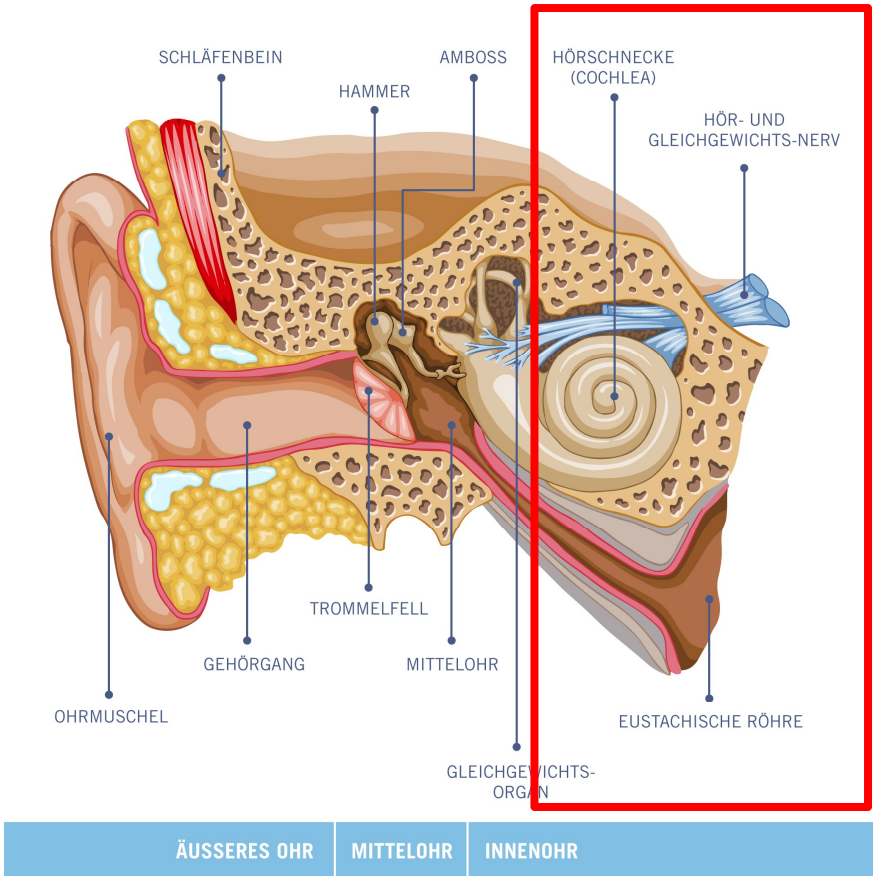
- Conductive hearing loss
  - Blockage of the ear canal
  - Damage or infection in the middle ear
- Sensorineural hearing loss
  - Damage to the cochlea
  - Damaged auditory nerve



Quelle: https://www.hoersysteme.ch

Hearing Loss in the Inner Ear and Brain

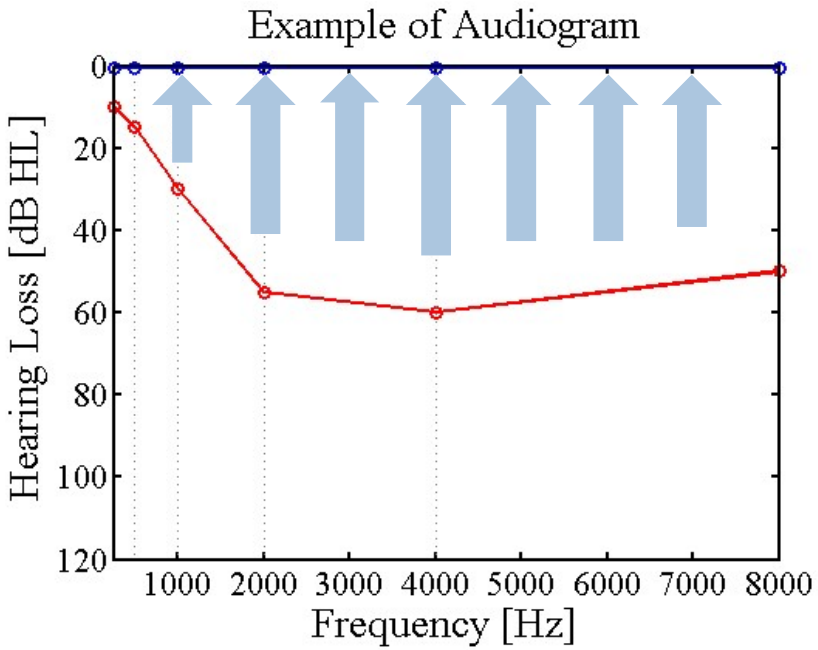
- Neural hearing loss
  - Damaged auditory nerve (non-genetic or genetic reasons)
- Central hearing loss
  - Disturbed perception processing of auditory stimuli in the brain



Quelle: https://www.hoersysteme.ch

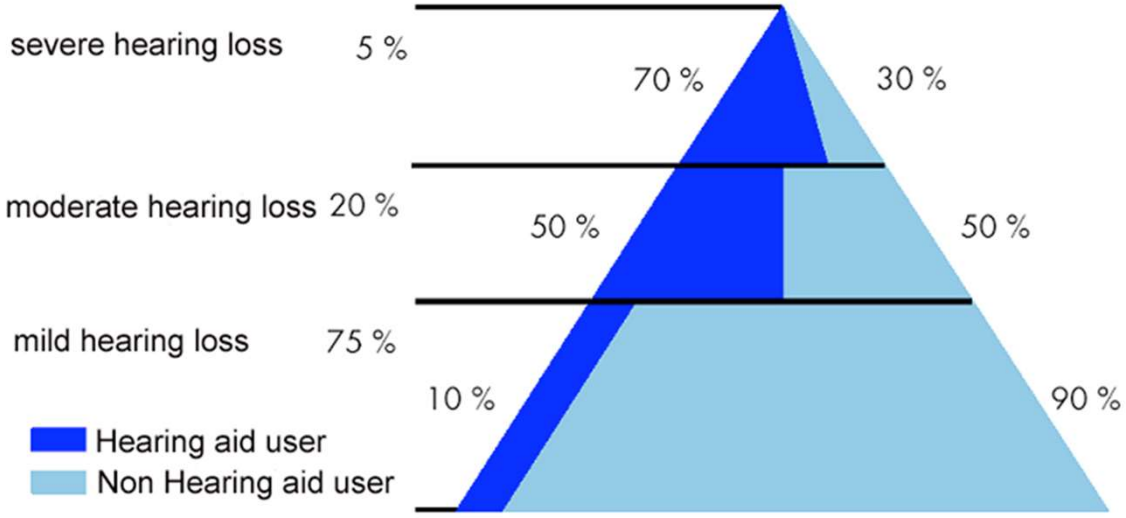
Hearing Aids against Hearing Loss

- Hearing aids can compensate for hearing loss in many cases
- An individual adjustment to the needs and complaints of a user is necessary and possible.



Hearing Loss and Hearing Aids

- From 2000 to 2015, the number of Americans with hearing loss has doubled. Globally the number is up by 44%. [1]
- Reduced speech intelligibility in complex acoustic scenarios with noise
- The consequences are difficulties with social interaction and at work
- Treatment: Hearing aid devices



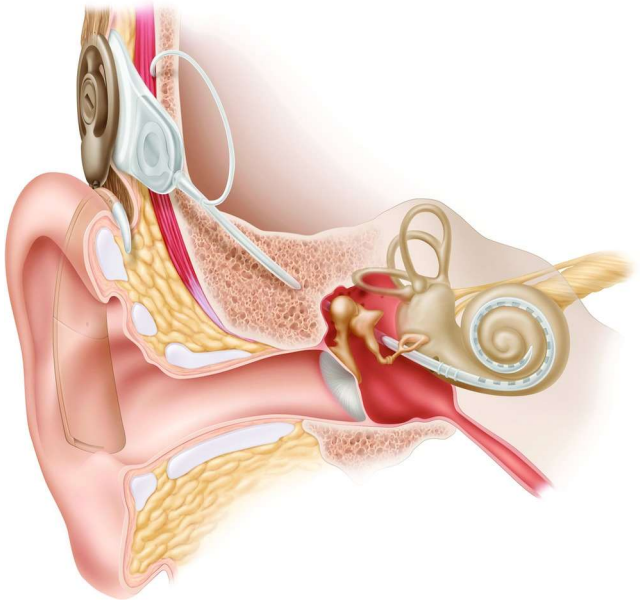
source: Phonak, ZKB

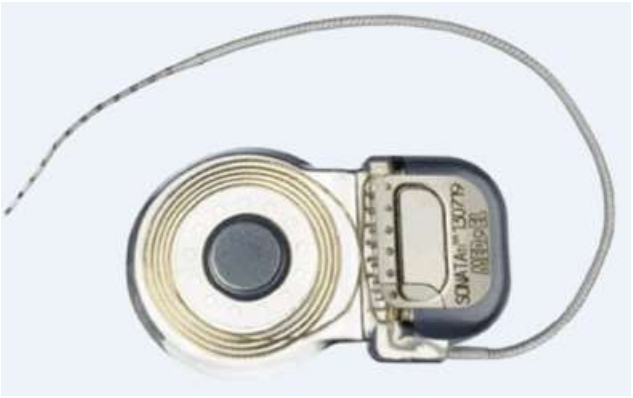
[1] Hearing Health Foundation (2016): HEARING LOSS & TINNITUS STATISTICS

Hearing Health Foundation
Prevention | Research | Cure

Cochlear Implant

- Consisting of 2 components
  - Processor
  - Implant
- Processor usually worn behind the ear
- Implant placed under the skin

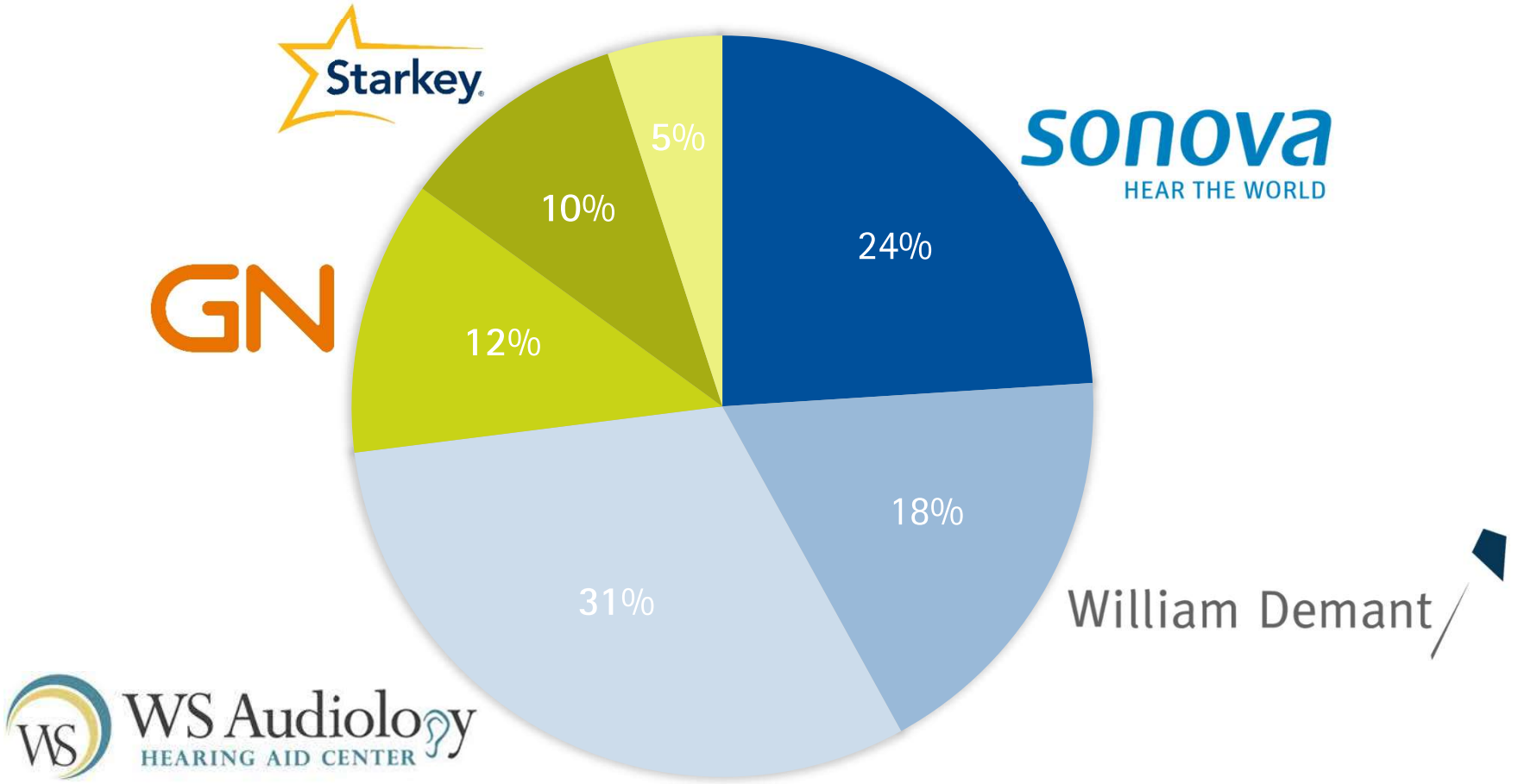




Quelle: DPA

Market shares of the largest hearing aid companies

- Market volume: ~6 billion US dollars



Quelle: Finanz und Wirtschaft |Schweiz

Cochlear Implant Manufacturer

- Market volume: ~3 billion US dollars

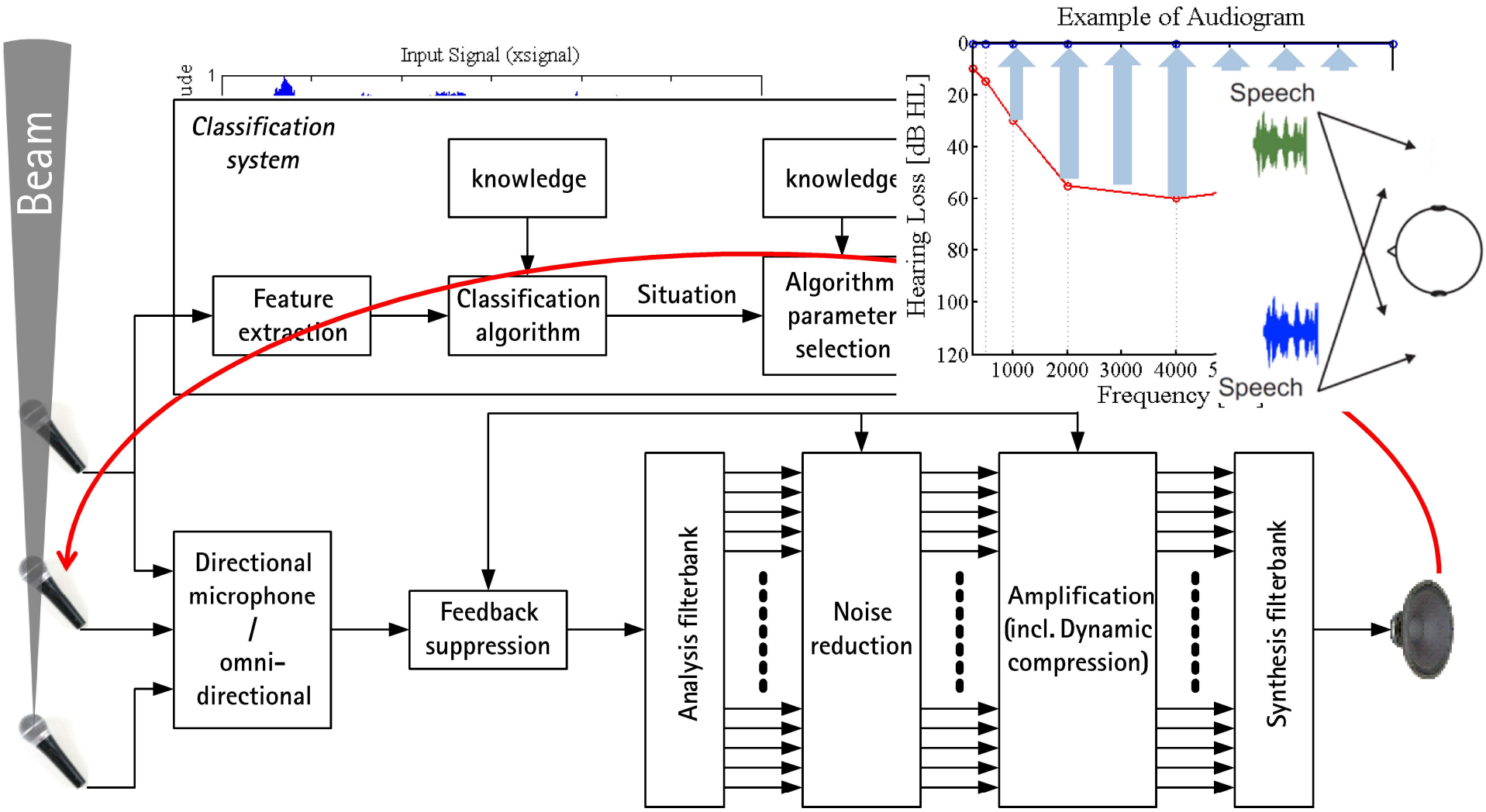
Cochlear®

MED-EL

oticon MEDICAL

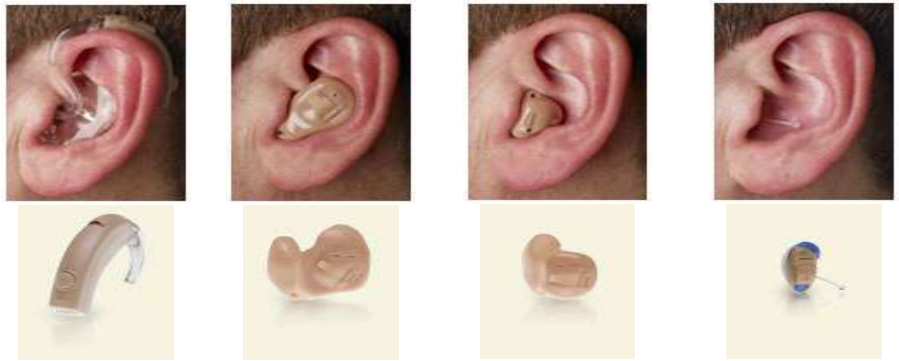
AB Advanced Bionics

Signal Processing in High-End Hearing Aids Systems

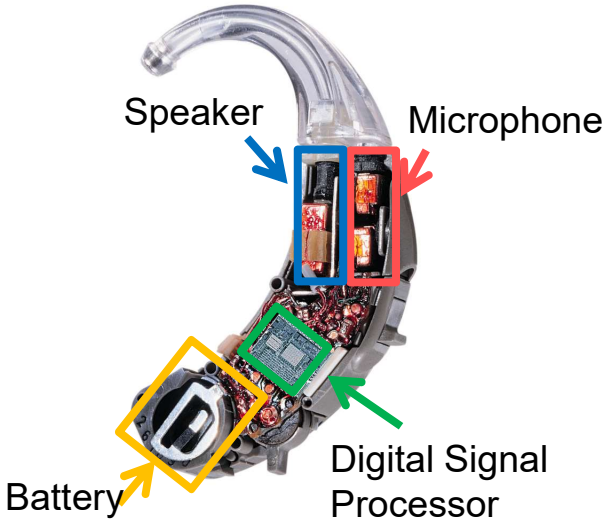


Digital Hearing Aid Systems

- Hearing aid technology requirements
  - Low-power: ~*1 mW* (longer battery lifetime)
  - Low processing delay: <*10 ms*
  - Small form factor (higher user acceptance)
  - Processing performance (algorithms)
  - Programmability / flexibility

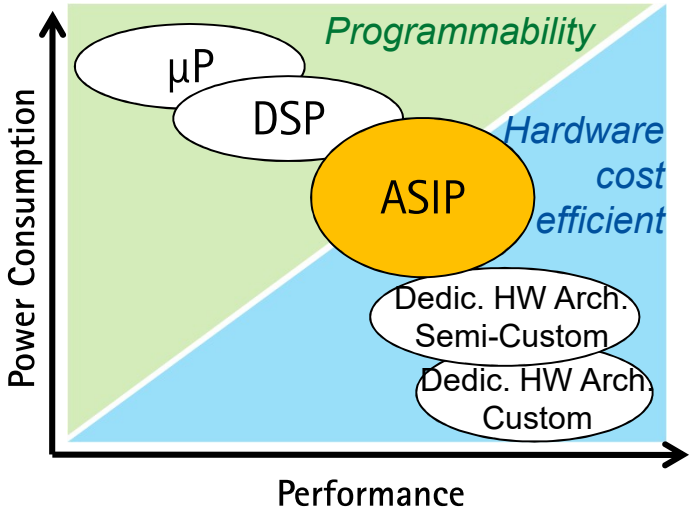


Behind The Ear (BTE) | In-The-Ear (ITE) | In-The-Canal (ITC) | Completely-In-Canal (CIC)



Application Specific Instruction-Set Processor for Hearing Aids

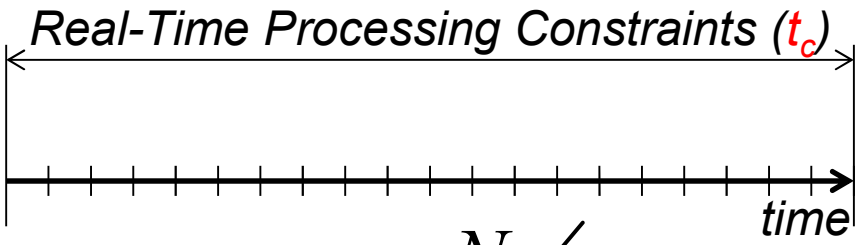
- Exploring the **application specific instruction set processor concept** for hearing aid systems
  - ISA, data path width, pipelining, ...
- Evaluating **low-power hardware accelerators** and design methodologies
  - Co-processors, custom hardware, ...
- **Power Optimization**
  - Power modeling and power-aware compiler/scheduler techniques



Low-Power Hearing Aid ASIPs

RISC Processor

$$A_a$$



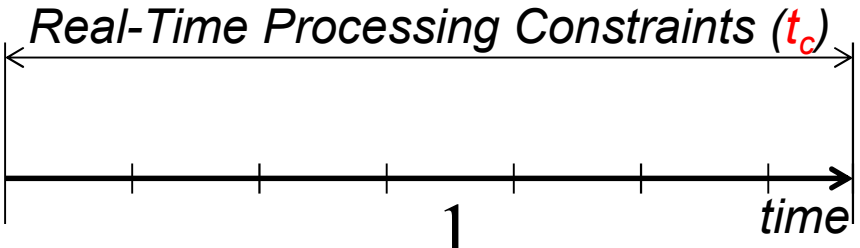
$$f_a = N / t_c$$

$$P_{dyn,a} = \sigma \cdot f_a \cdot C_a \cdot U^2$$

+ Custom FUs

RISC Processor

$$A_b = 2 \cdot A_a$$

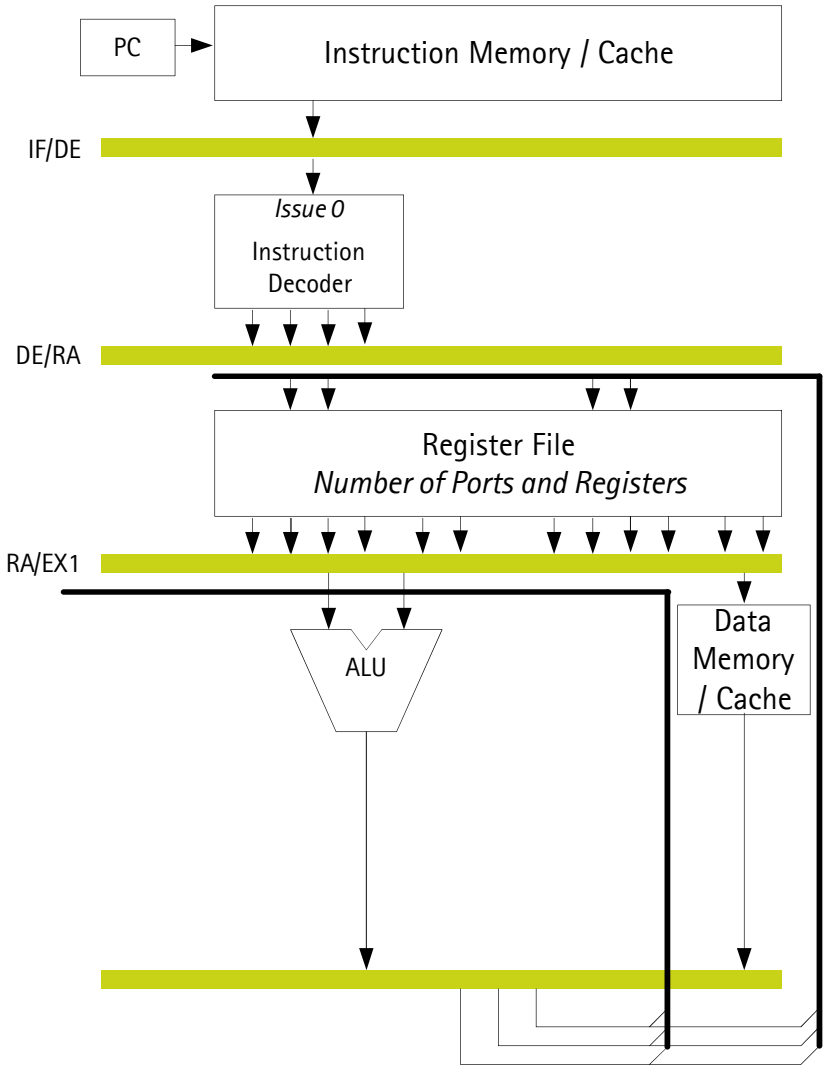


$$f_b = \frac{1}{4} \cdot f_a$$

$$P_{dyn,b} = \frac{1}{2} \cdot \sigma \cdot f_a \cdot C_a \cdot U^2$$

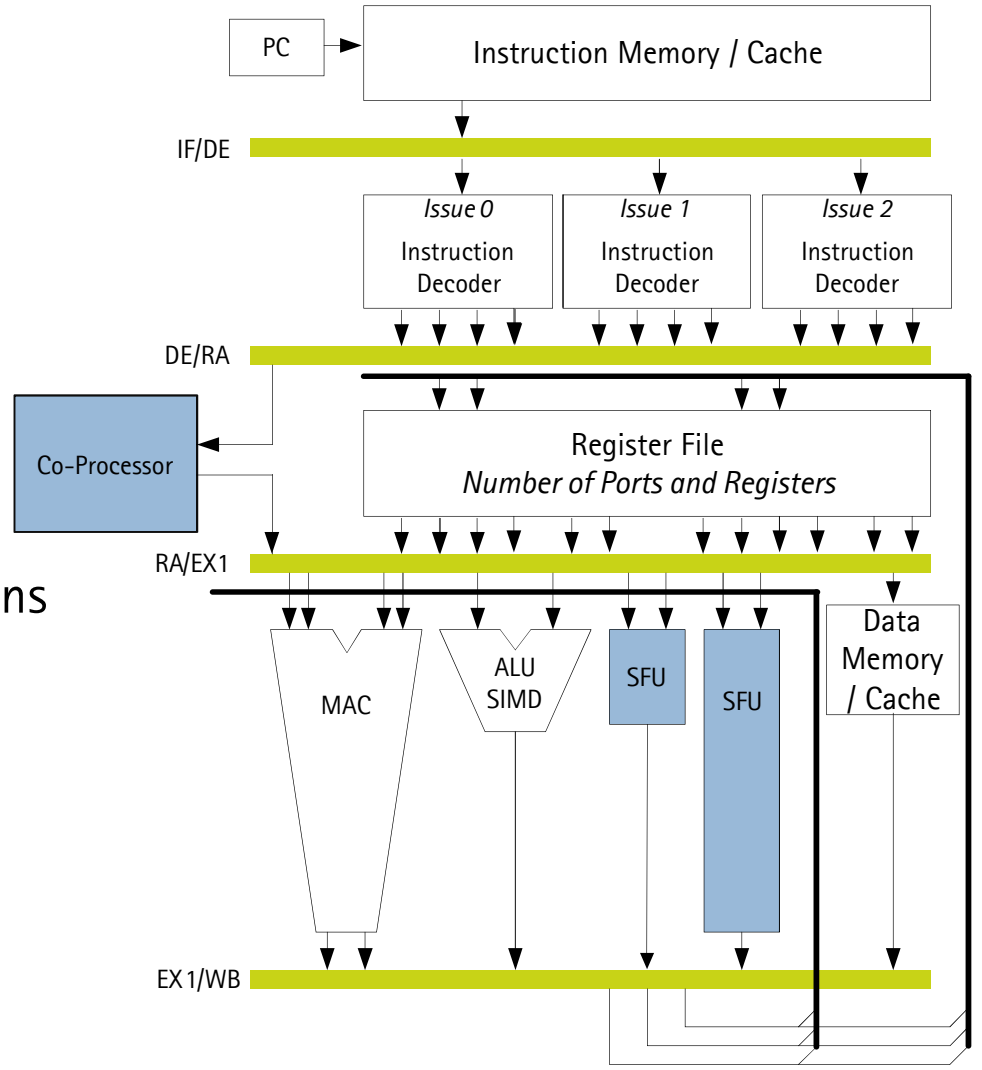
Application Specific Instruction-Set Processor

- Baseline Architecture



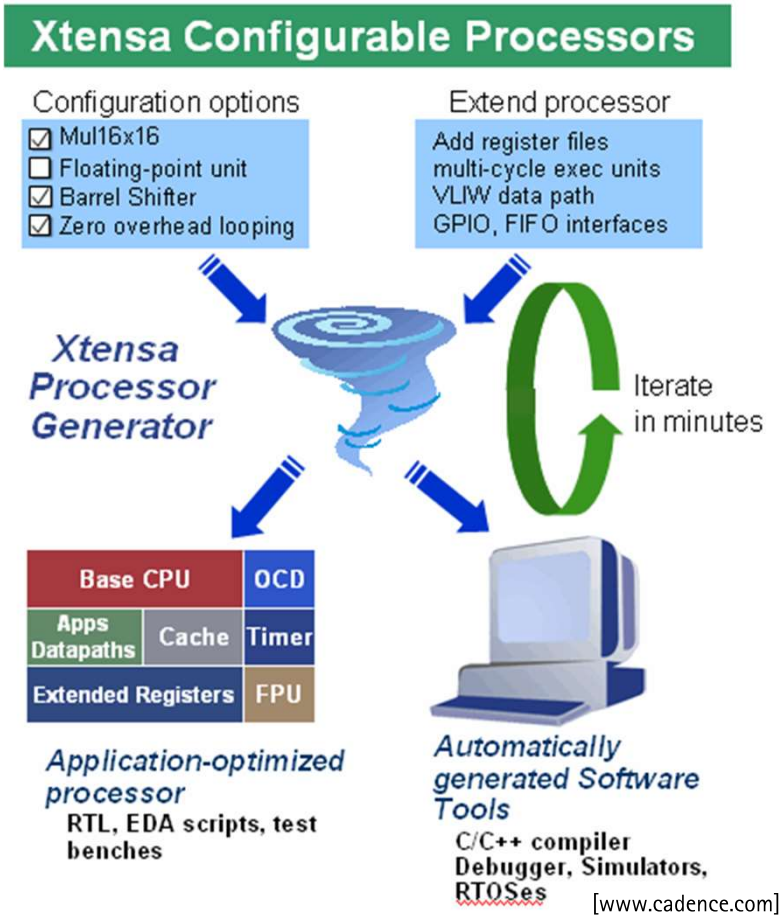
Application Specific Instruction-Set Processor

- Baseline Architecture
- Basic Architecture Parameters
  - Register File Configuration
  - Memory System
  - Instruction-Set Architecture
- Parallelization Techniques
  - Number of Parallel Instructions
  - SIMD / Subword Parallelism
- Specialization Techniques
  - Custom Instructions
  - Co-processor Architectures
- Compiler / Software Support



Xtensa Customizable Processor / Cadence

- Baseline Architecture
  - Reduced 32-bit ISA, 5 pipeline stages
  - 16 KB Instruction Cache and 16 KB Memory Cache
- Configurable
  - Caches, bus width, GP register file, MUL, MAC, INT, number of load/store units
- Expandable
  - New instruction, register, ports
  - Using TIE language (similar to Verilog)



➢ Area and energy optimization are possible

Extension of the Xtensa Processor with hardware units

- Using TIE language (Tensilica Instruction Extension)
  - Custom instructions, registers and interfaces
  - Can be used in the C program code
  - SIMD-example: 4x 16bit additions

Definition of a custom instruction

vec4_add16.tie

```
regfile simd64 64 16 v     // 16 x 64bit Register
operation vec4_add16 {out simd64 sum, in simd64 A, in simd64 B} {} {
          wire [15:0] result0 = (A[15: 0] + B[15: 0]);
          wire [15:0] result1 = (A[31:16] + B[31:16]);
          wire [15:0] result2 = (A[47:32] + B[47:32]);
          wire [15:0] result3 = (A[63:48] + B[63:48]);
          assign sum = {result3, result2, result1, result0}; }
```

Using the custom instruction in C

use_vec4_add16.c

```
#include <xtensa/tie/vec4_add16.h>
simd64 A[VECLEN];
simd64 B[VECLEN];
simd64 sum[VECLEN];
for (i=0; i<VECLEN; i++)
          sum[i] = vec4_add16(A[i],B[i]);
```

Xtensa Customizable Processor / Cadence

- Configuration Implemented for the HA System
  - Baseline (1-Issue-Slot)
  - Baseline (2-Issue-Slots)
  - Baseline (3-Issue-Slots)

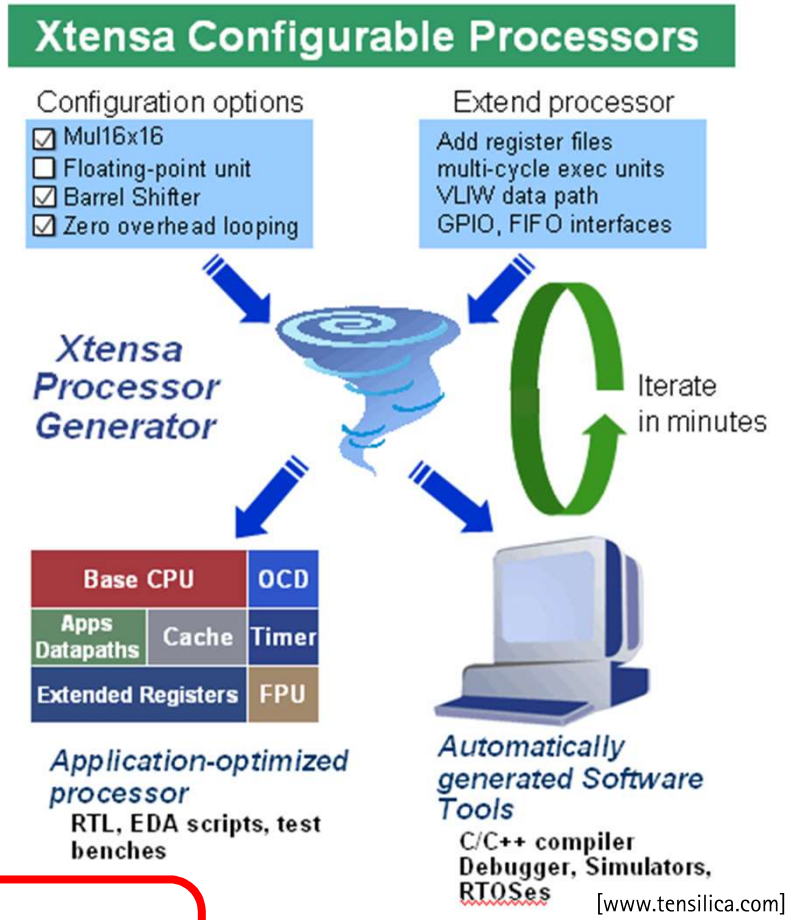
  Exploring parallelism

  - Customized (1-Issue-Slot)

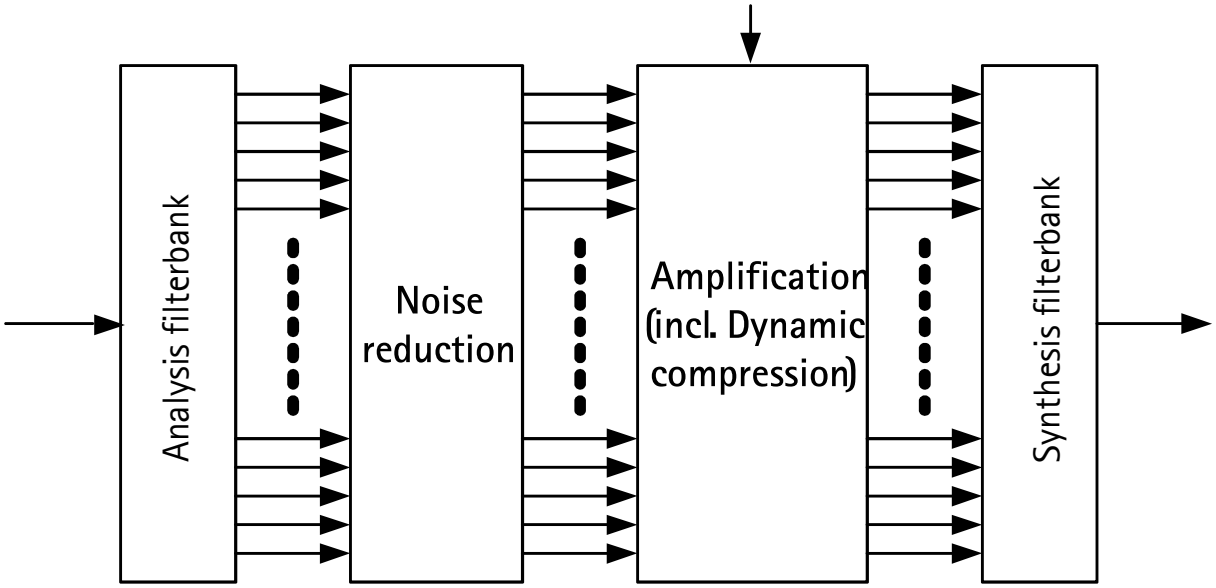
  Exploring specialization

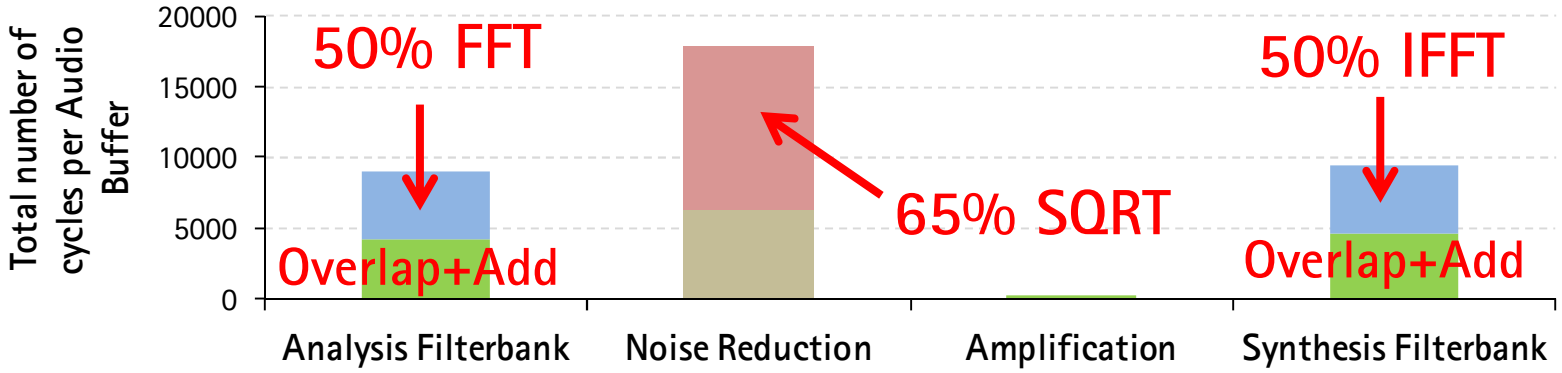
  - Customized (2-Issue-Slots)

  Exploring parallelism and specialization



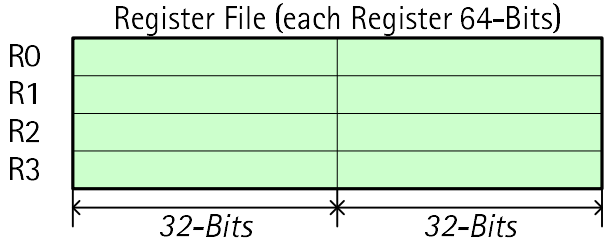
Customized Configuration: Complex Instruction Extensions

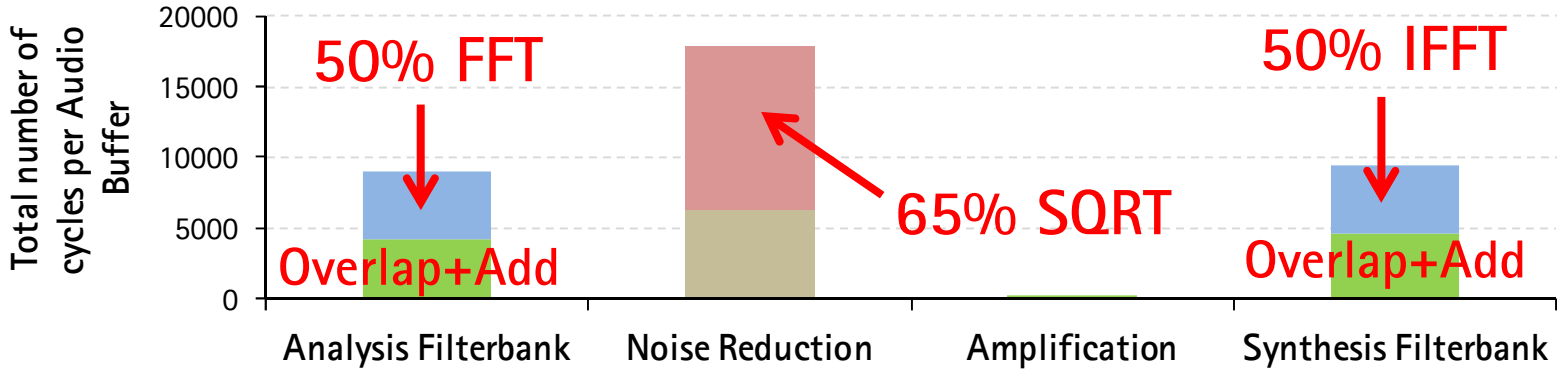




Customized Configuration: Complex Instruction Extensions

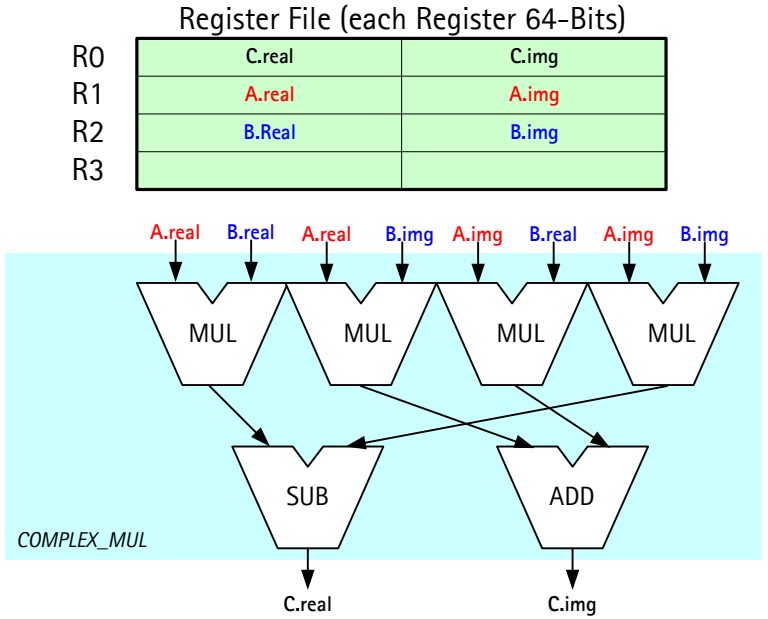
- New Register File for SIMD-Op.

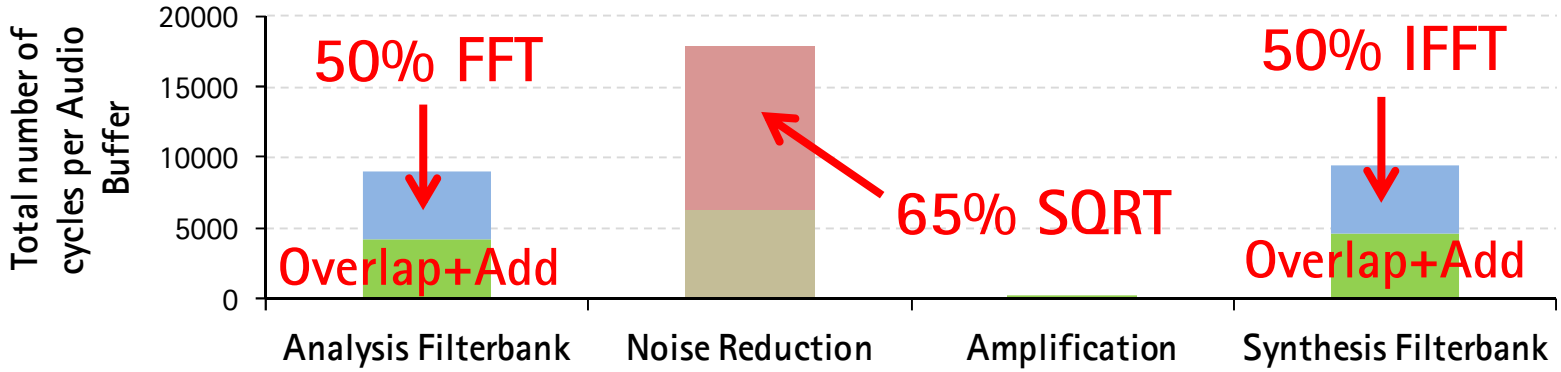




Customized Configuration: Complex Instruction Extensions

- New Register File for SIMD-Op.
- **COMPLEX ARITHMETIC** Op.
  - R0 = COMPLEX_ADD(R1,R2)
  - R0 = COMPLEX_MUL(R1,R2)
  - R0 = COMPLEX_CONJ(R1)
  - AR0 = BIT_REVERSE(AR1)





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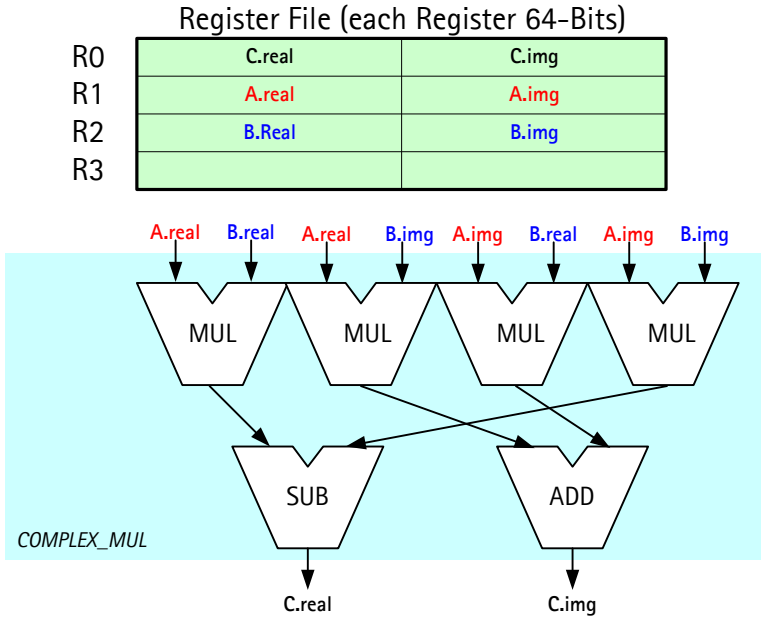
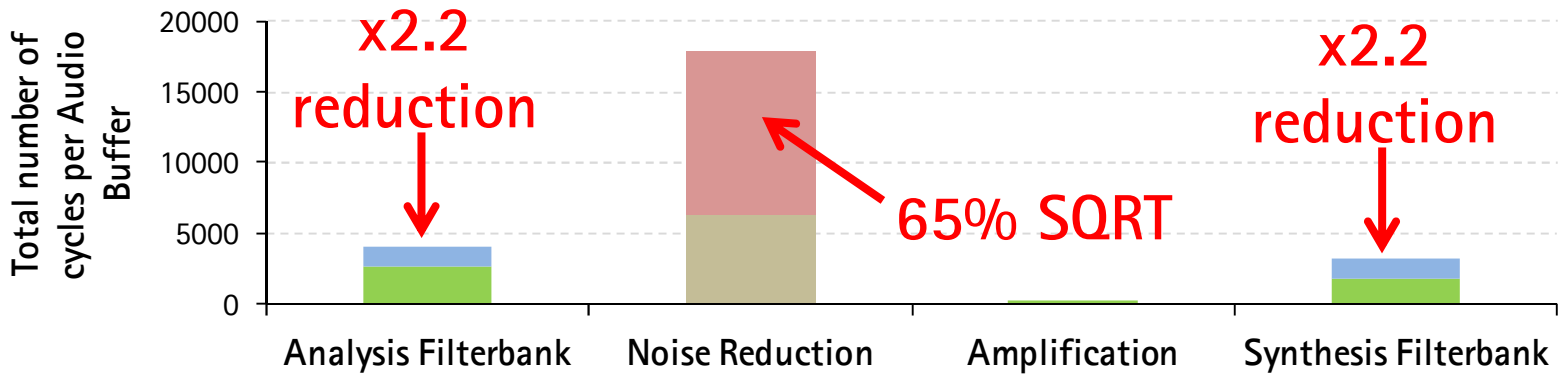
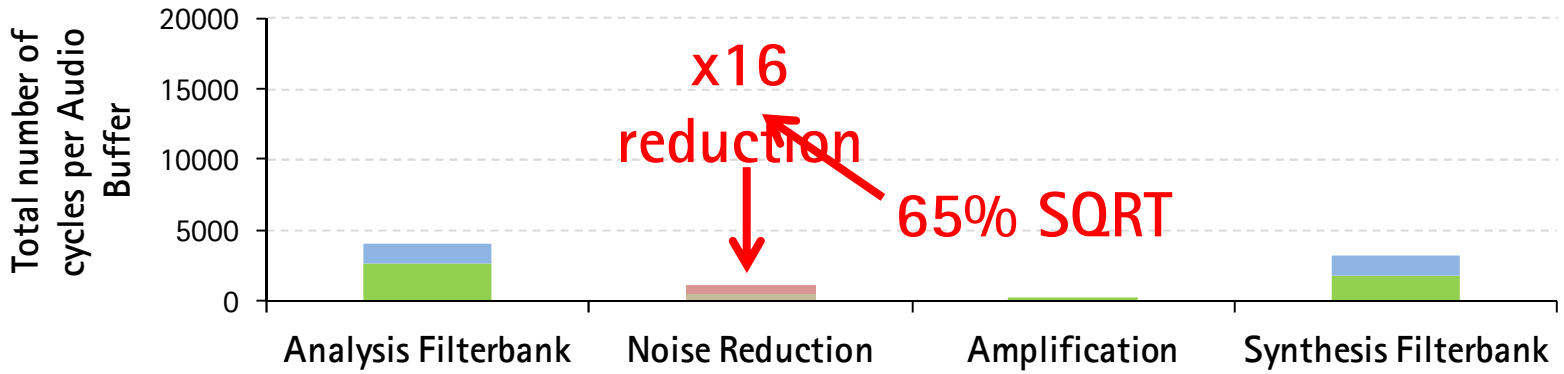




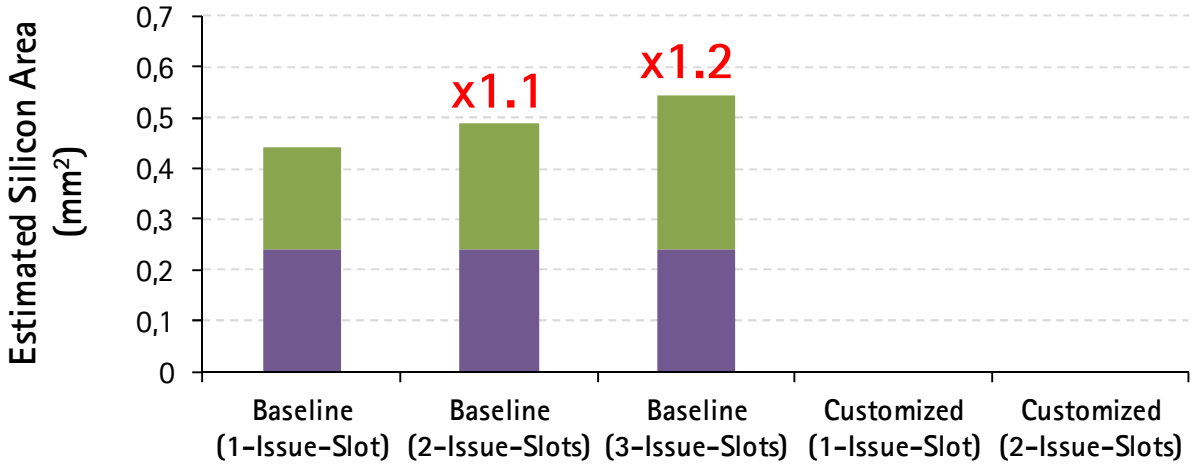
Customized Configuration: Complex Instruction Extensions

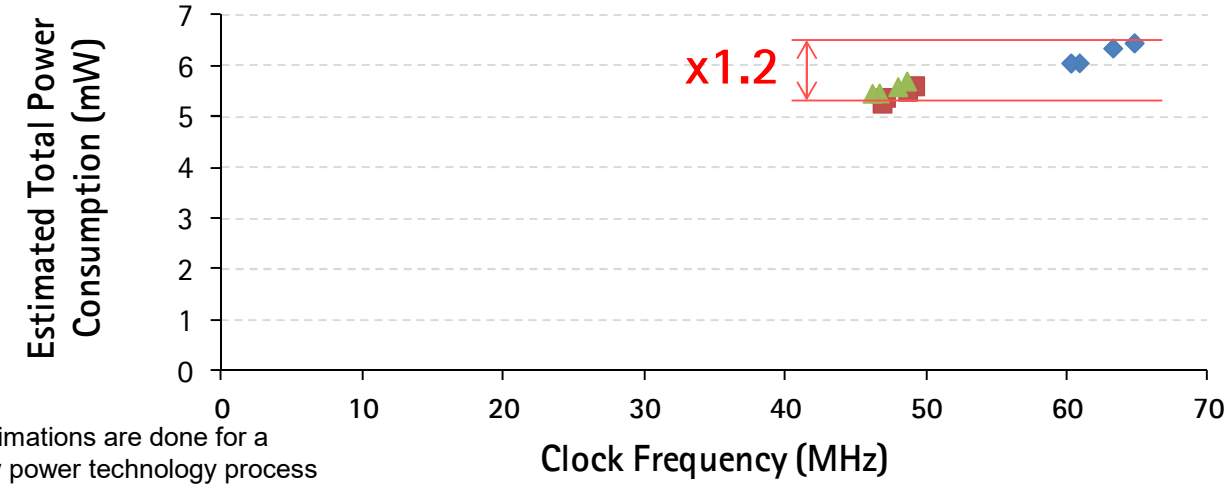
- **SQRT** Operations
  - LEADING_ONES(R0)
  - R0 = SQUARE_ROOT(R1)
  - R0 = THRESHOLD(R0,R1,R2)

Newton-Raphson method for square root computation



Exemplary Hearing Aid Processing – ASIP Design Space Exploration

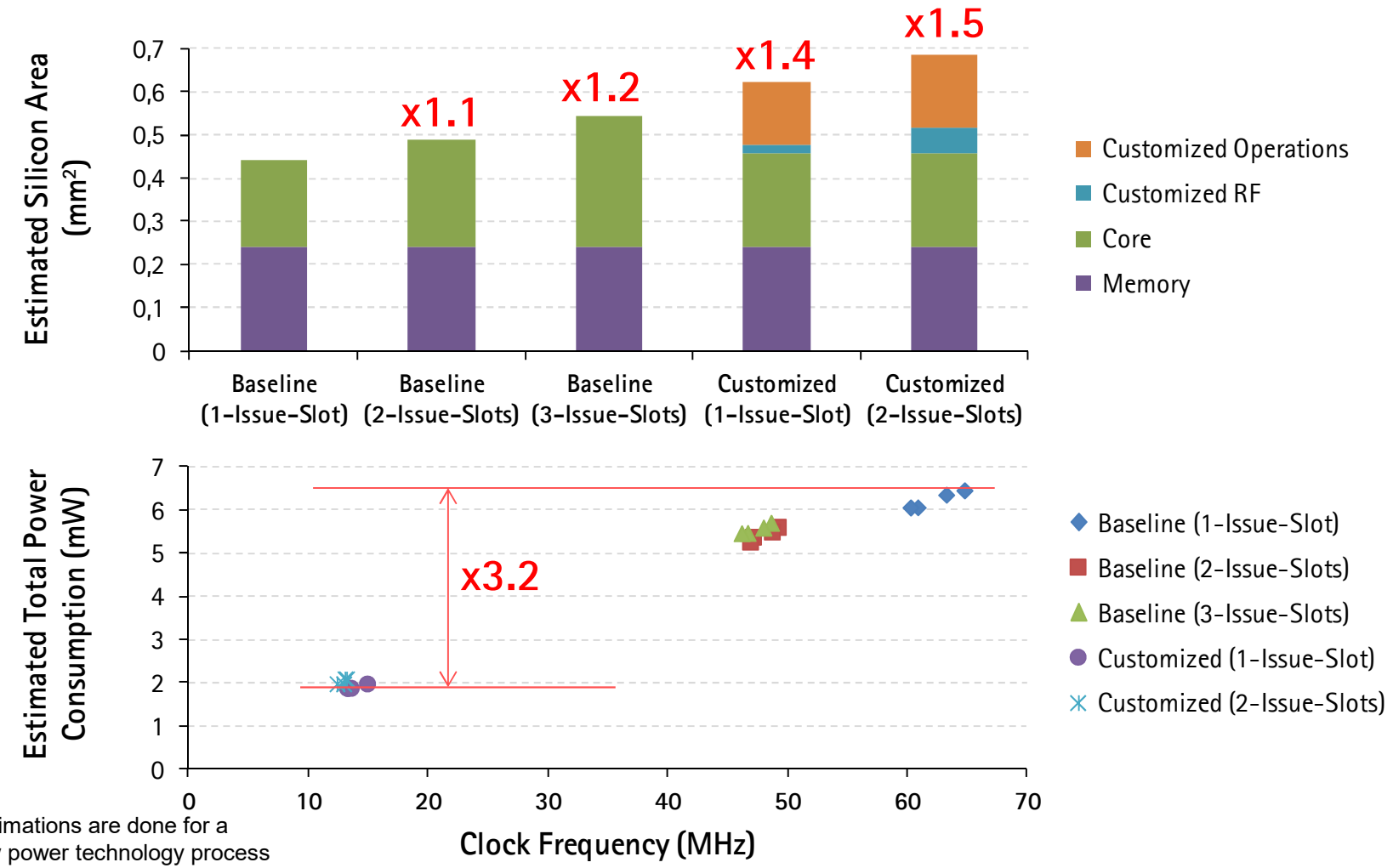




These estimations are done for a 40 nm low power technology process

[Werner; Payá Vayá, Blume, *"Case Study: Using the Xtensa LX4 Configurable Processor for Hearing Aid Applications"*, ICT.OPEN 2013]

Exemplary Hearing Aid Processing – ASIP Design Space Exploration

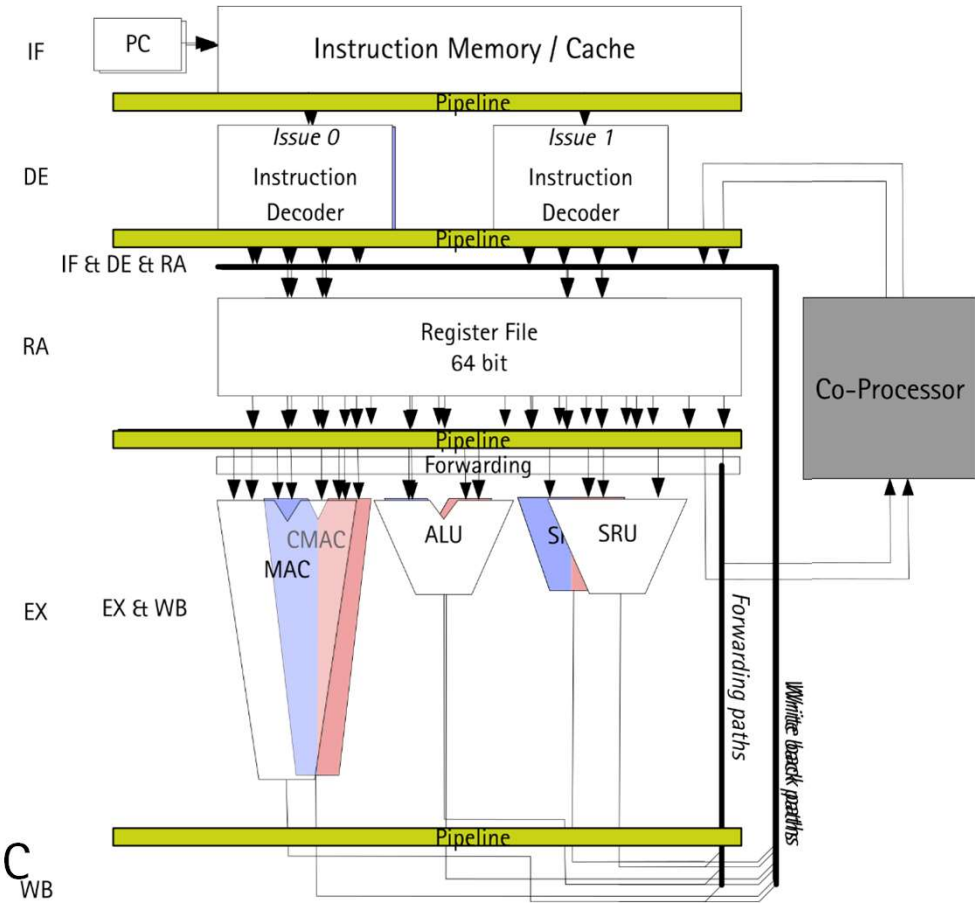


These estimations are done for a 40 nm low power technology process

Baseline KAVUAKA Architecture

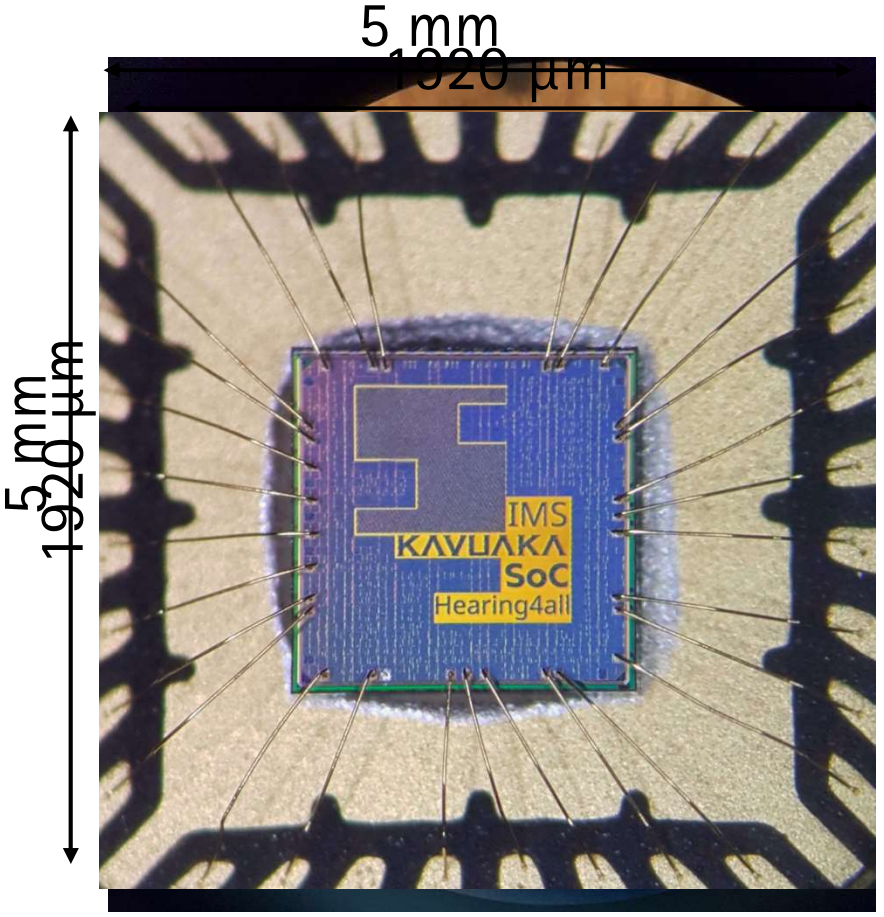
- ASIP Processor Architecture
- Basic Generic Parameters
  - Pipeline Stages
  - Bitwidth (64/48/32/24 bit)
- Parallelization Techniques
  - SIMD Subword Parallelism
  - VLIW Instruction Parallelism
- Specialization Techniques
  - Complex-valued MAC
  - Co-Processors
  - Instruction Merge (X2)
  - Idle Operation

➢ 4 configurations selected for the SoC



KAVUAKA Hearing Aid Processor System-on-Chip

- The manufactured KAVUAKA hearing aid System-on-Chip
  - 40 nm TSMC LP technology
  - 3.6 mm^2 chip area
  - 0.8 million standard cells
  - 28 SRAM memories
    - 4x 2048x64-bit
    - 4x 1024x64-bit
    - 4x 1024x48-bit
    - 16x 512x16-bit
  - 37 input/output cells
  - 8 metal layers



Close-up of the chip
Chip in a QFN package
with approx. 125x magnification.

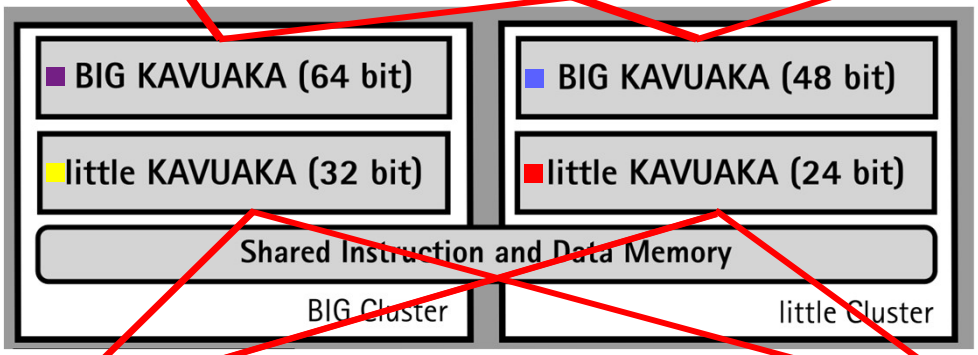
KAVUAKA ASIP configurations

SIMD instructions + Complex multiply accumulate MAC (CMAC)

- 1x64 bit, 2x32 bit, 4x16 bit and 8x8bit
- 1x48 bit, 2x24 bit and 4x12 bit

Instruction Merge (X2)

- Functional units duplicated Load/Store up to 256 bit
- Functional units duplicated Load/Store up to 192 bit



Scalar instructions + Scalar MAC

- 1x32 bit
- 1x24 bit

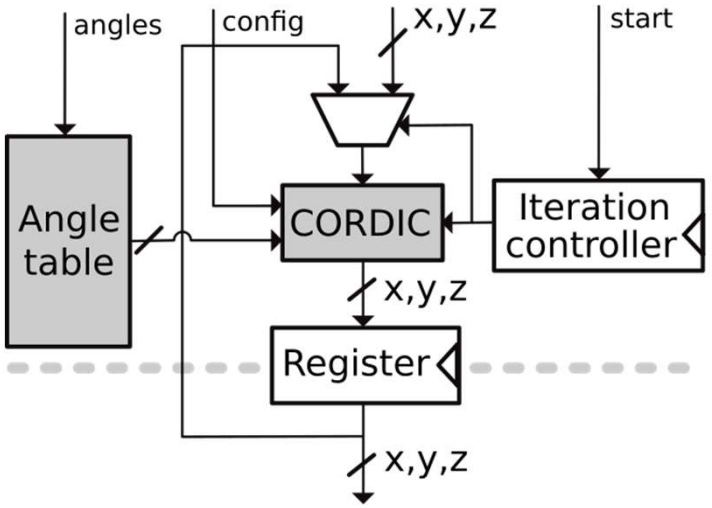
No Instruction Merge

- Load/Store up to 64 bit
- Load/Store up to 48 bit

Co-Processor Architecture

- Co-Processor Architecture
  - CORDIC (Coordinate Rotation Digital Computer)
- Generic parameters
  - Number of CORDIC kernel processing units
  - Single instruction multiple data (SIMD) operations

➢ 10 configurations selected for the SoC

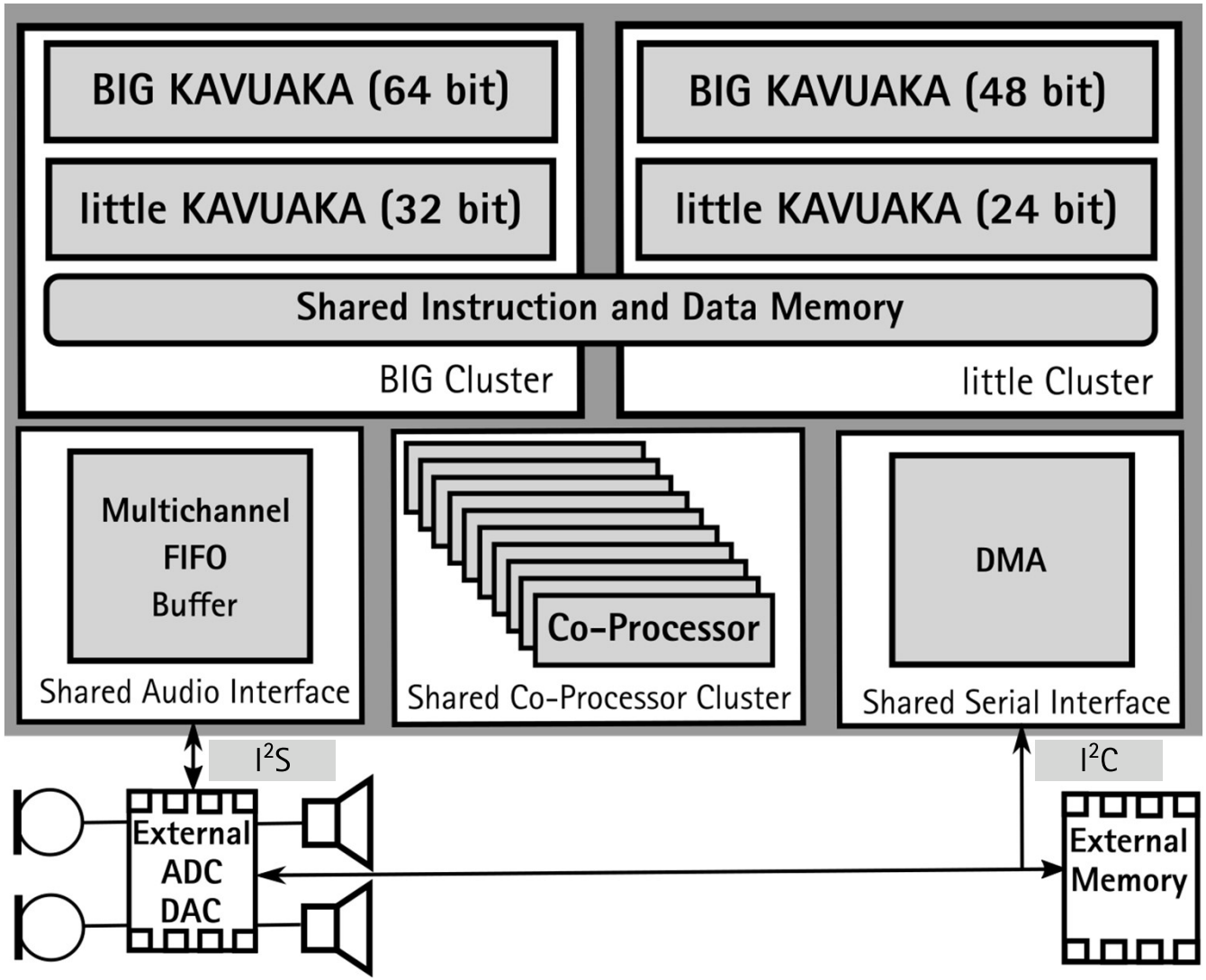


Example applications:

- Division: Normalized LMS Algorithm (Beamforming)
- Logarithm: Log power spectrum (Speech recognition)

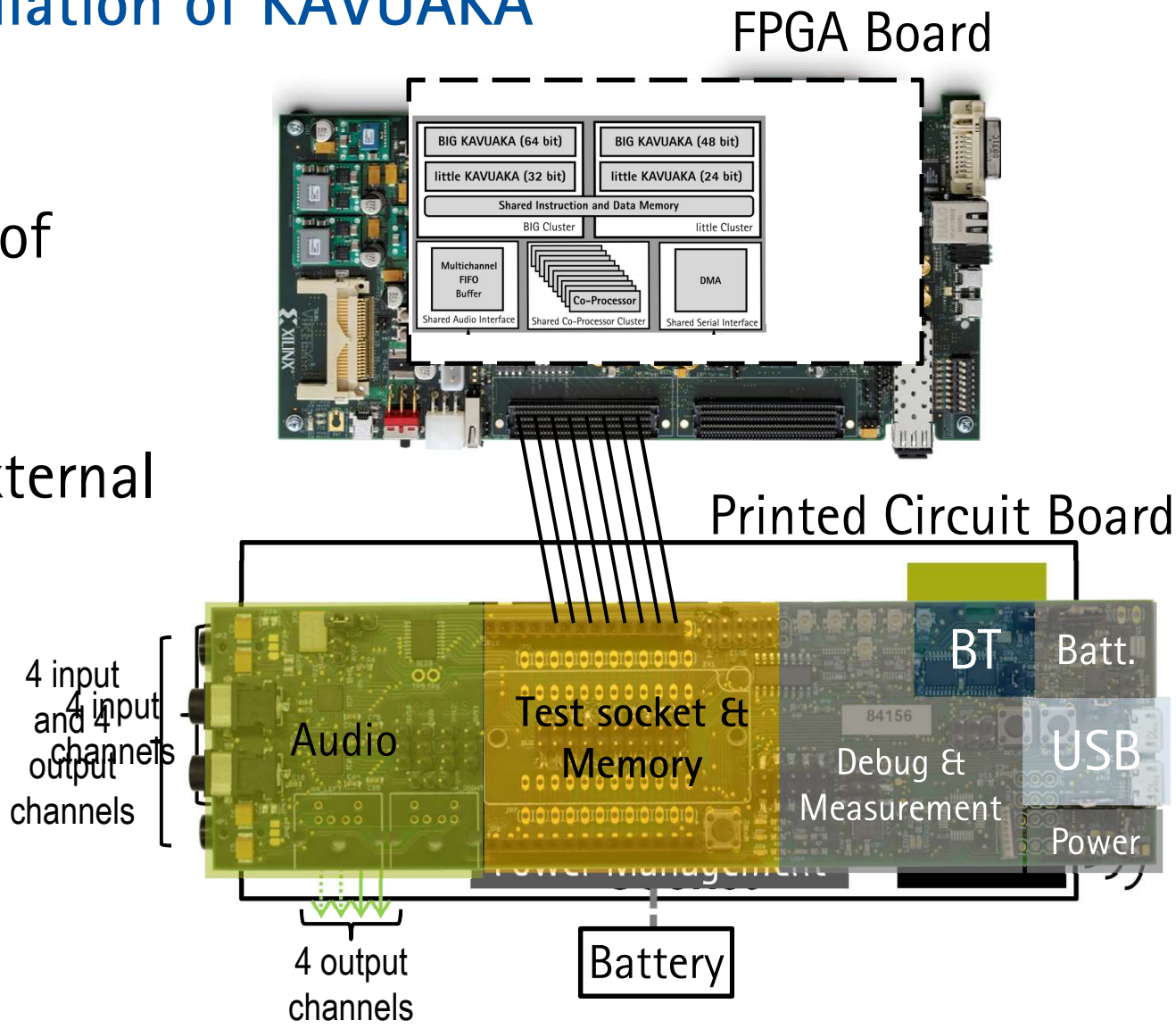
The System-on-Chip Architecture

System-on-Chip
with
4 **KAVUAKA**
cores and
10 co-processors



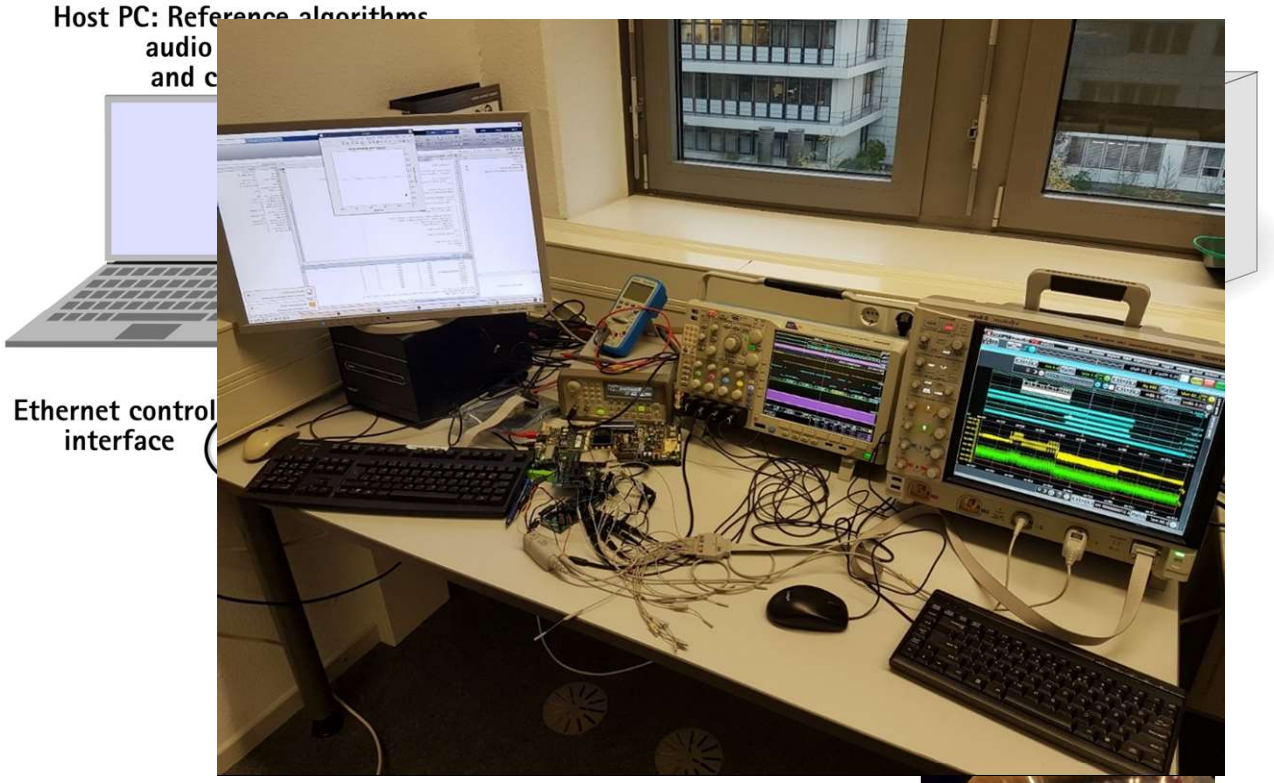
In-circuit Emulation of KAVUAKA

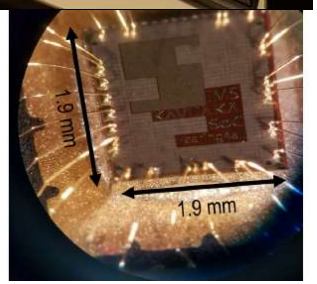
- Functional verification of the SoC
- Use real or emulated external components
- ASIC is placed on the test socket after tape-out



Setup for Power Measurements

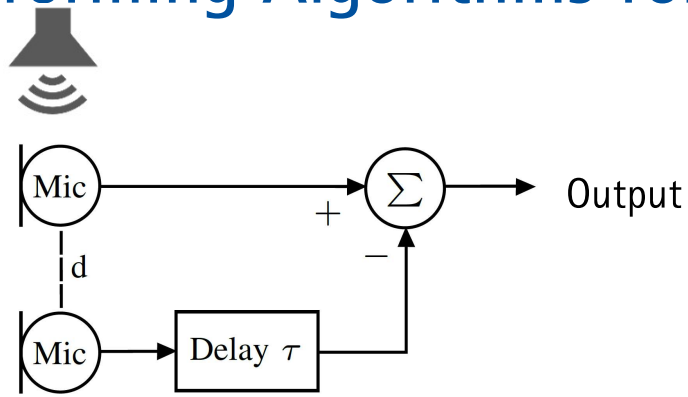
- Measure the power consumption for different hearing aid configurations and algorithms
- Automatic measurements including:
- Host PC for controlling and audio streaming
- Power supply and oscilloscopes controlled by PC
- FPGA emulation of external hearing aid components

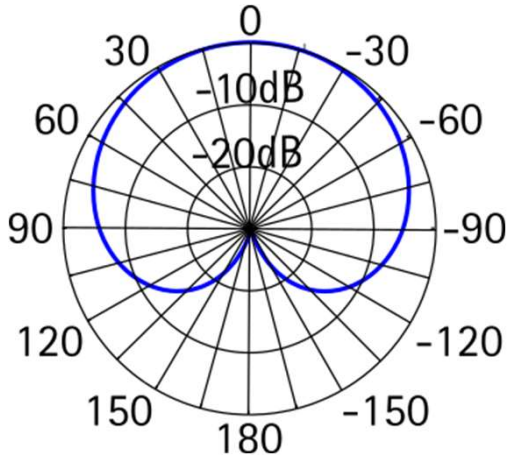




Beamforming Algorithms for Hearing Aids

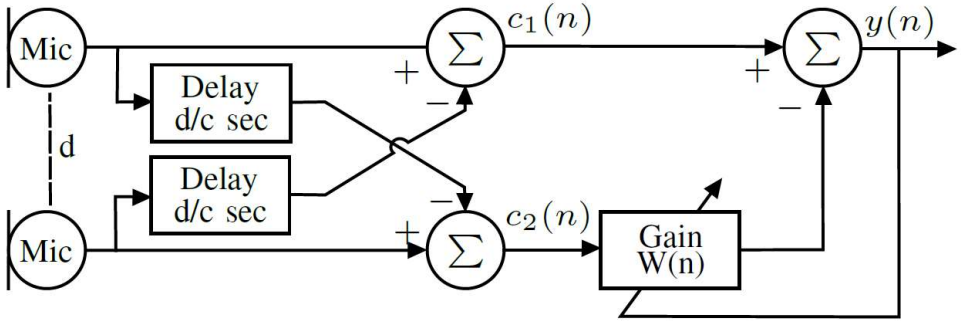
Fixed Beamformer



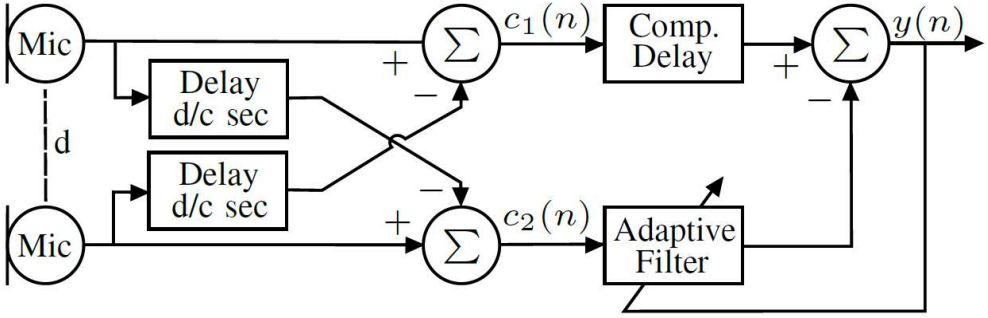


Output Polar Pattern

Adaptive Gain Beamformer

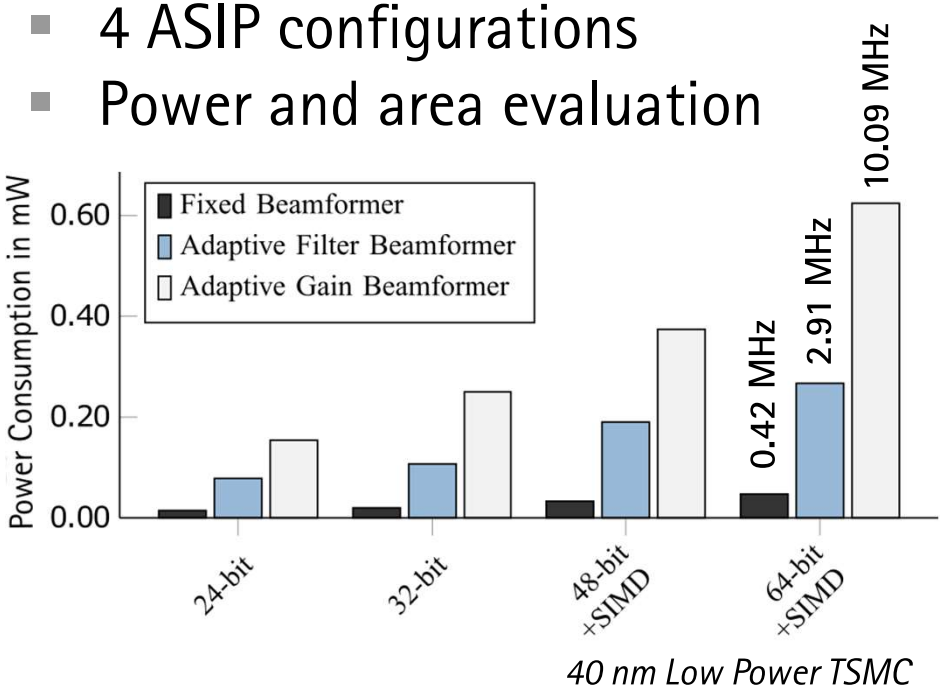


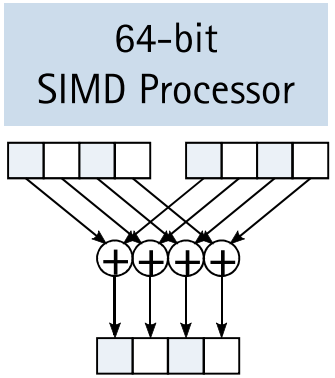
Adaptive Filter Beamformer

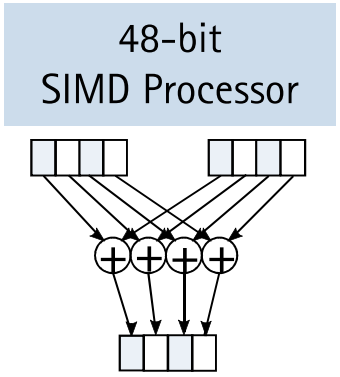


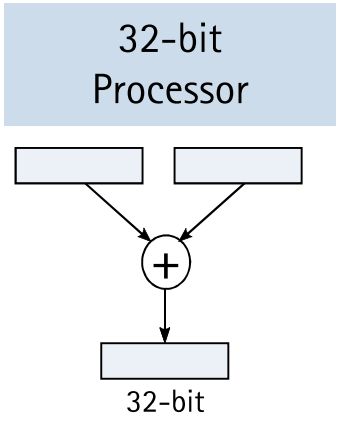
Results for Beamforming Algorithms on different ASIP configurations

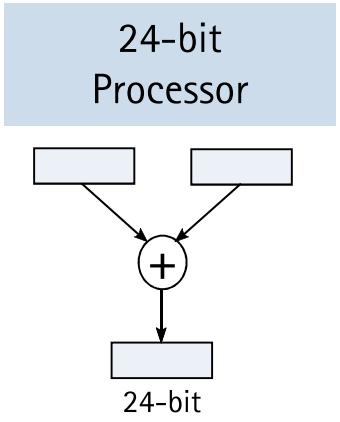
- Fixed and adaptive Beamforming algorithms
- 4 ASIP configurations
- Power and area evaluation





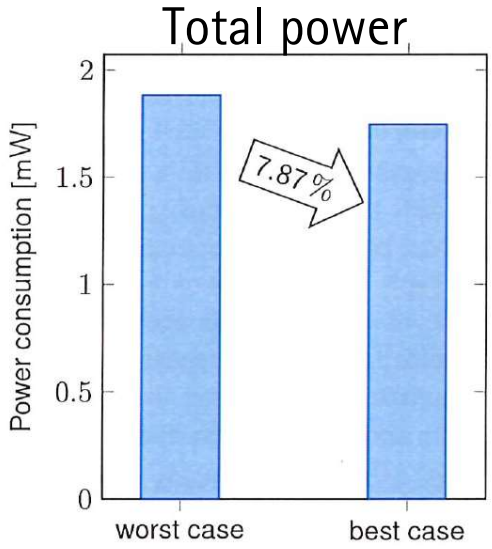






Power Optimization Based on an Accurate Power Model

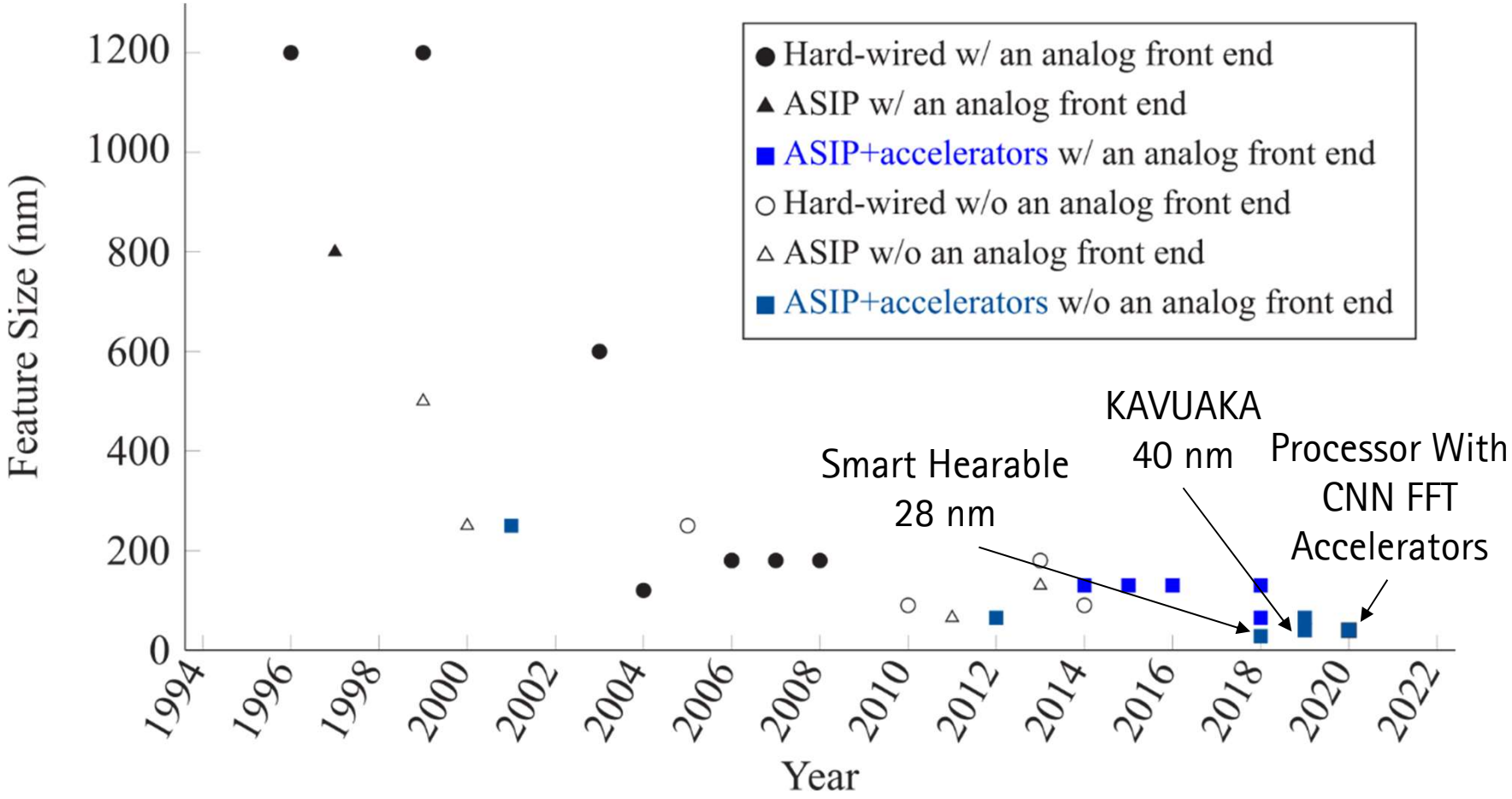
- Power optimization after manufacturing
- Exploit the flexibility offered by the ASIP architecture
  - During instruction scheduling and register allocation
- Register accesses cause high switching activity in the address decoder of the multi port register file



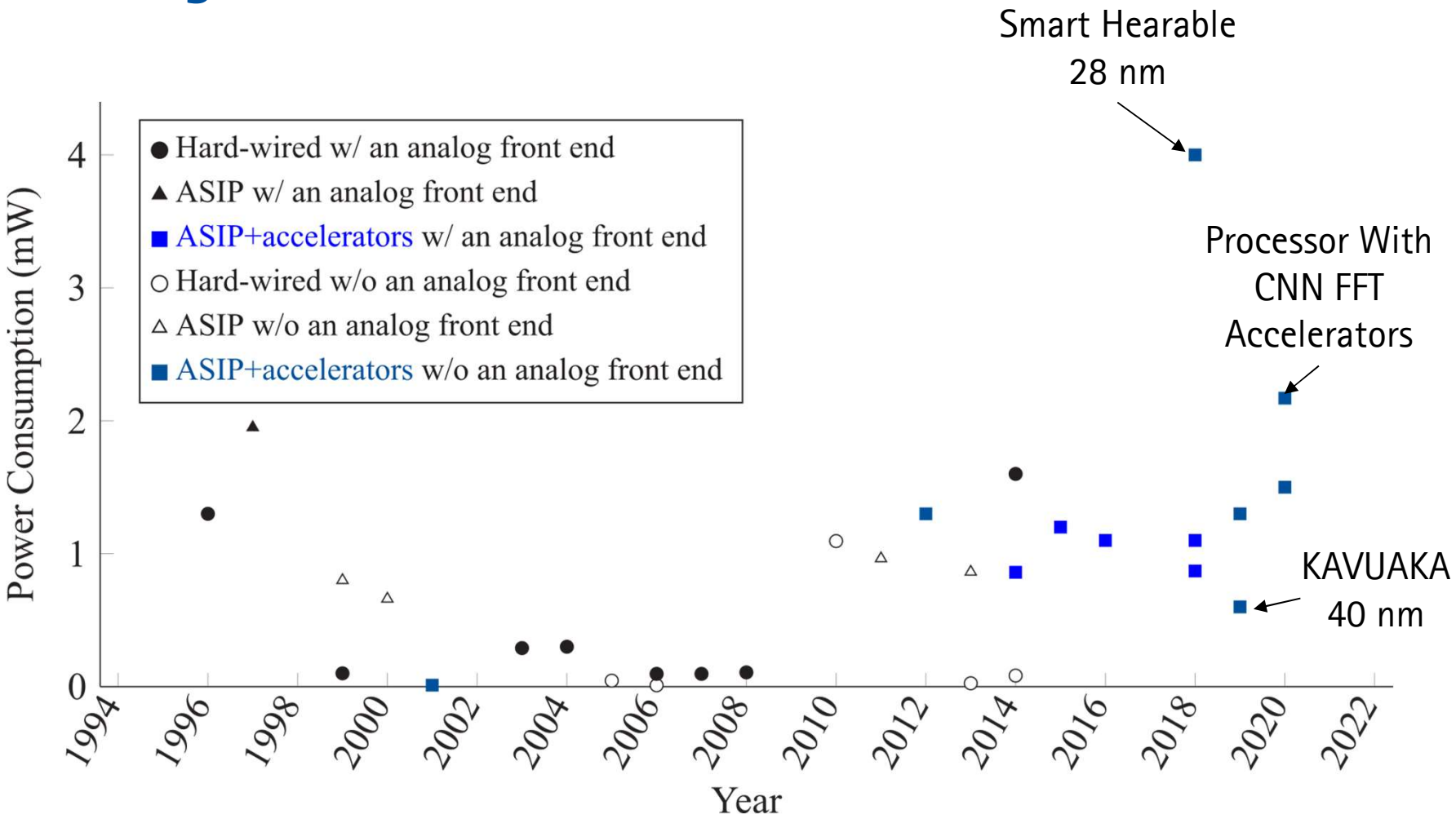
Register addressing of two consecutive instructions influences power consumption

Worst Case:	Best case:
ADD R0, R0, R0	ADD R0, R0, R0
ADD R31, R31, R31	ADD R0, R0, R0

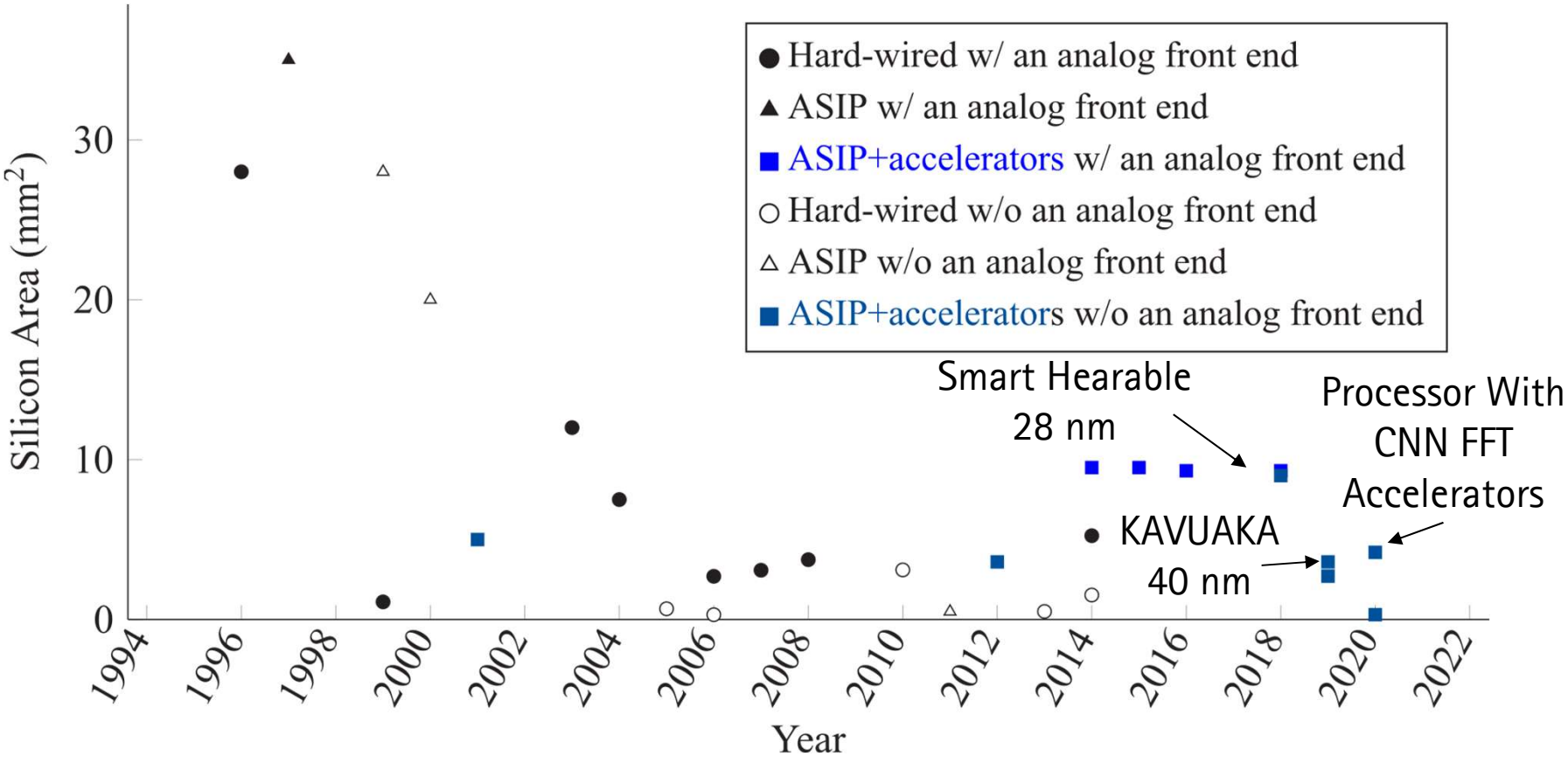
Feature Sizes of Commercial and Research Hearing Aids



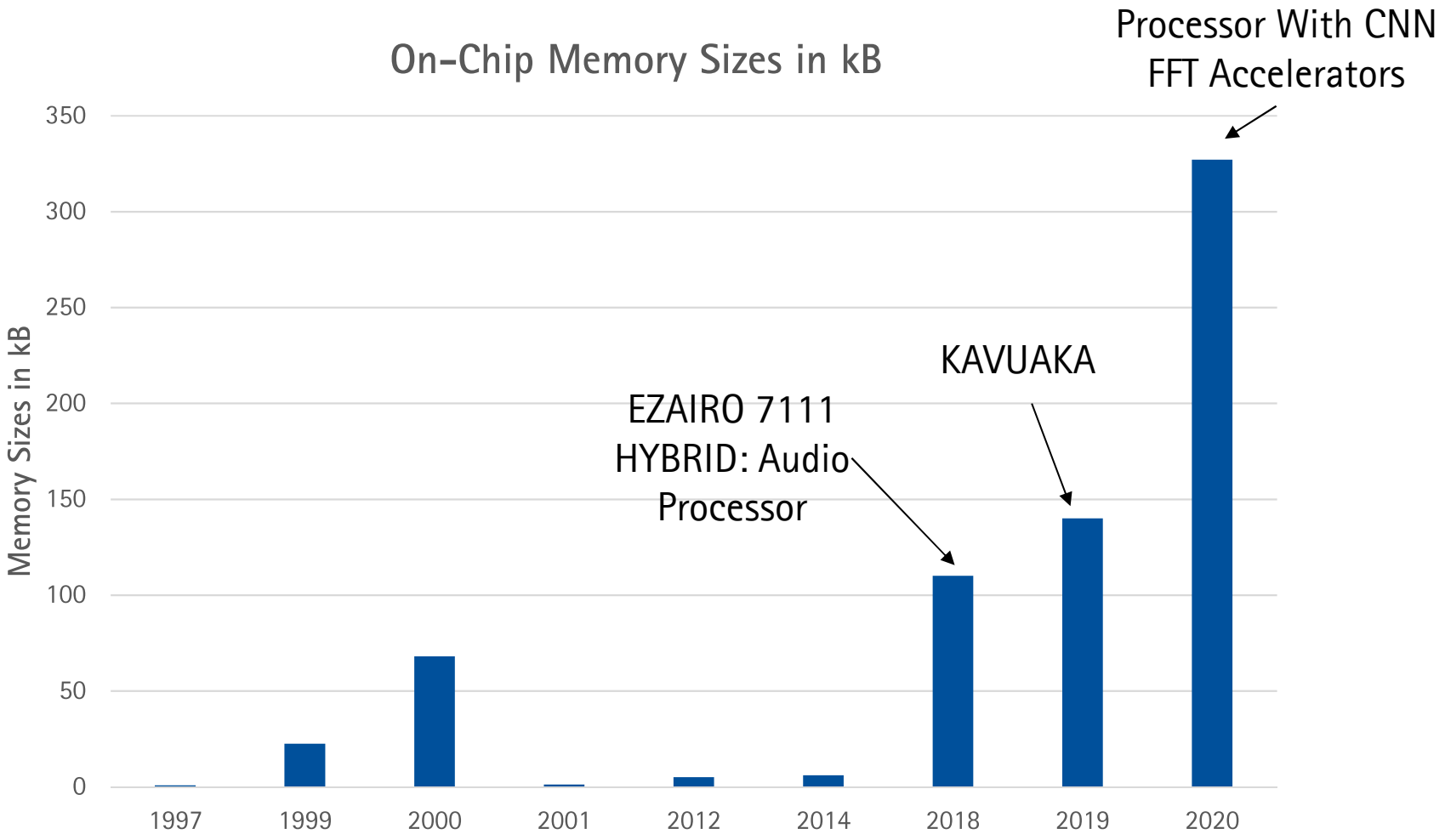
Power Consumption of Commercial and Research Hearing Aids



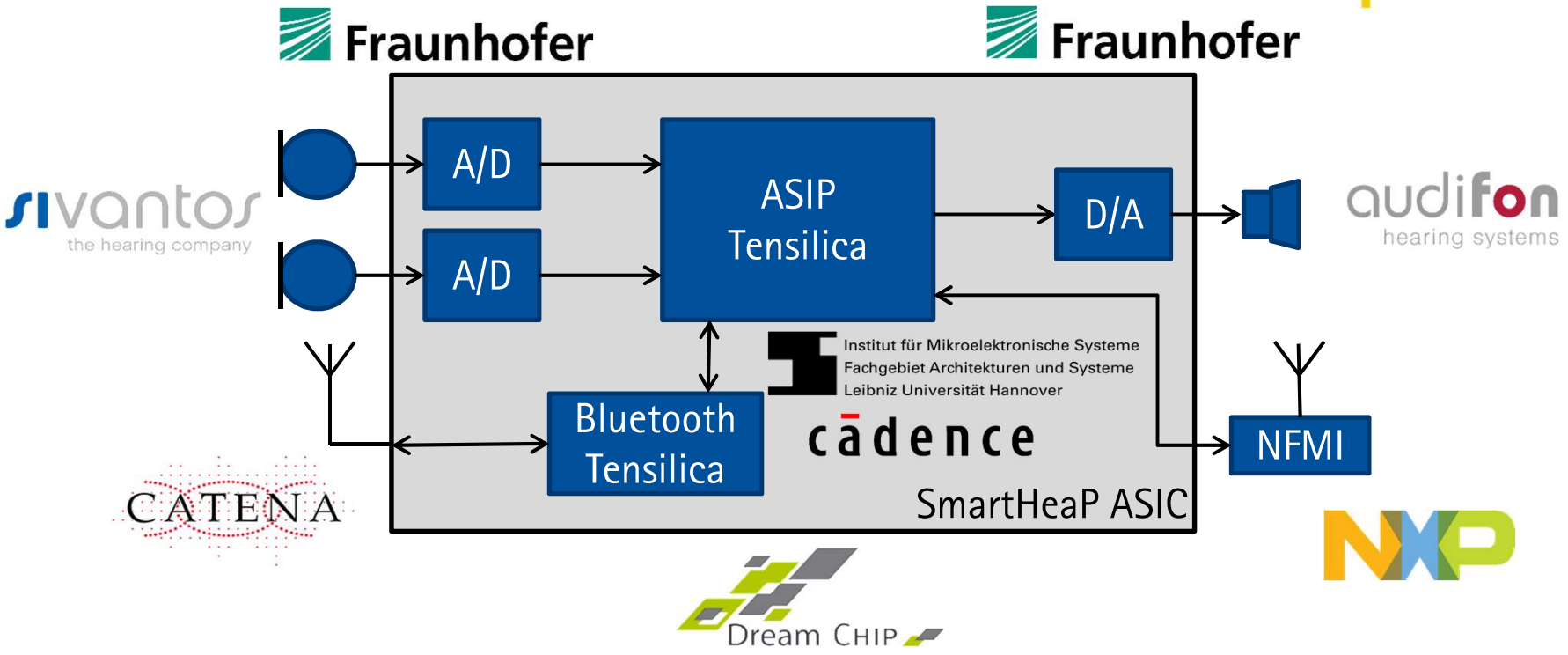
Silicon Area of Commercial and Research Hearing Aids



On-Chip Memory Sizes



Smart Hearing Aid Processor (SmartHeaP)
ASIC Concept



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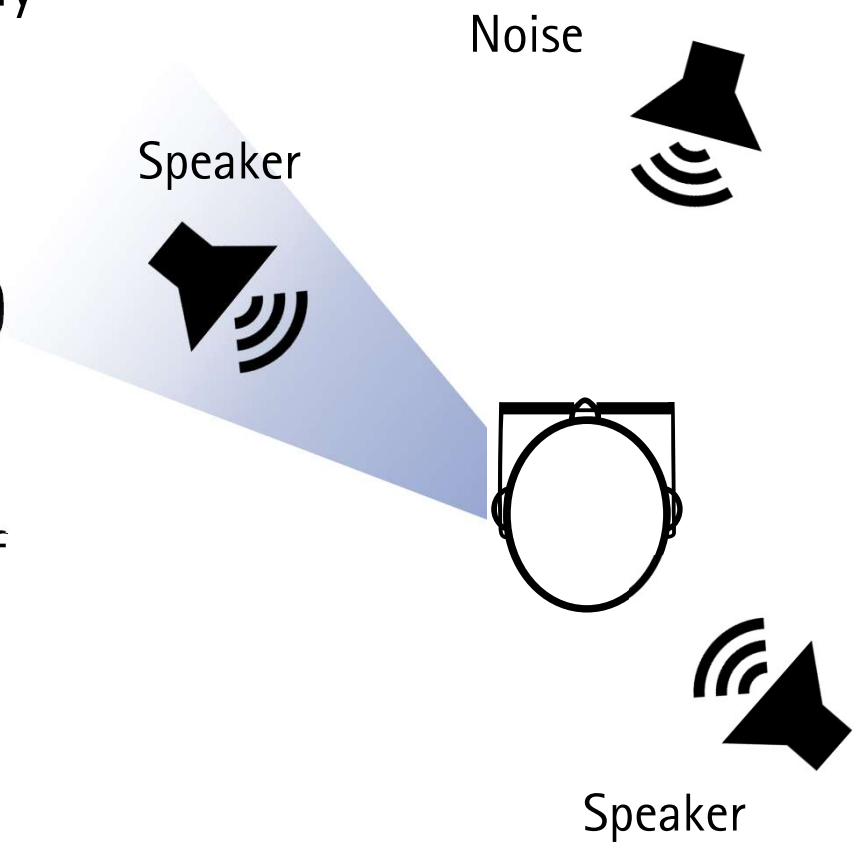
Reference algorithms

GLOBALFOUNDRIES

22 nm FDSOI

Applied Deep Learning in Hearing Aids

- Cocktail Party Scenario: many Speakers and Noise
- Advanced techniques available e.g. Beamformers, but Direction of Arrival(DOA) as input is needed [ICASSP 2020]
- ➢ Use CNN to estimate DOA of Speech



Conclusion

- Number of hearing impaired persons increases
  - New hearing aids are necessary
- Strict constrains, like power consumption or processing performance
- KAVUAKA – a hearing aid ASIP from the IMS
  - Design process and verification
  - Post silicon evaluation and optimization
- Further trends in hearing aid research
  - Accelerators for neural networks
  - EEG signal processing